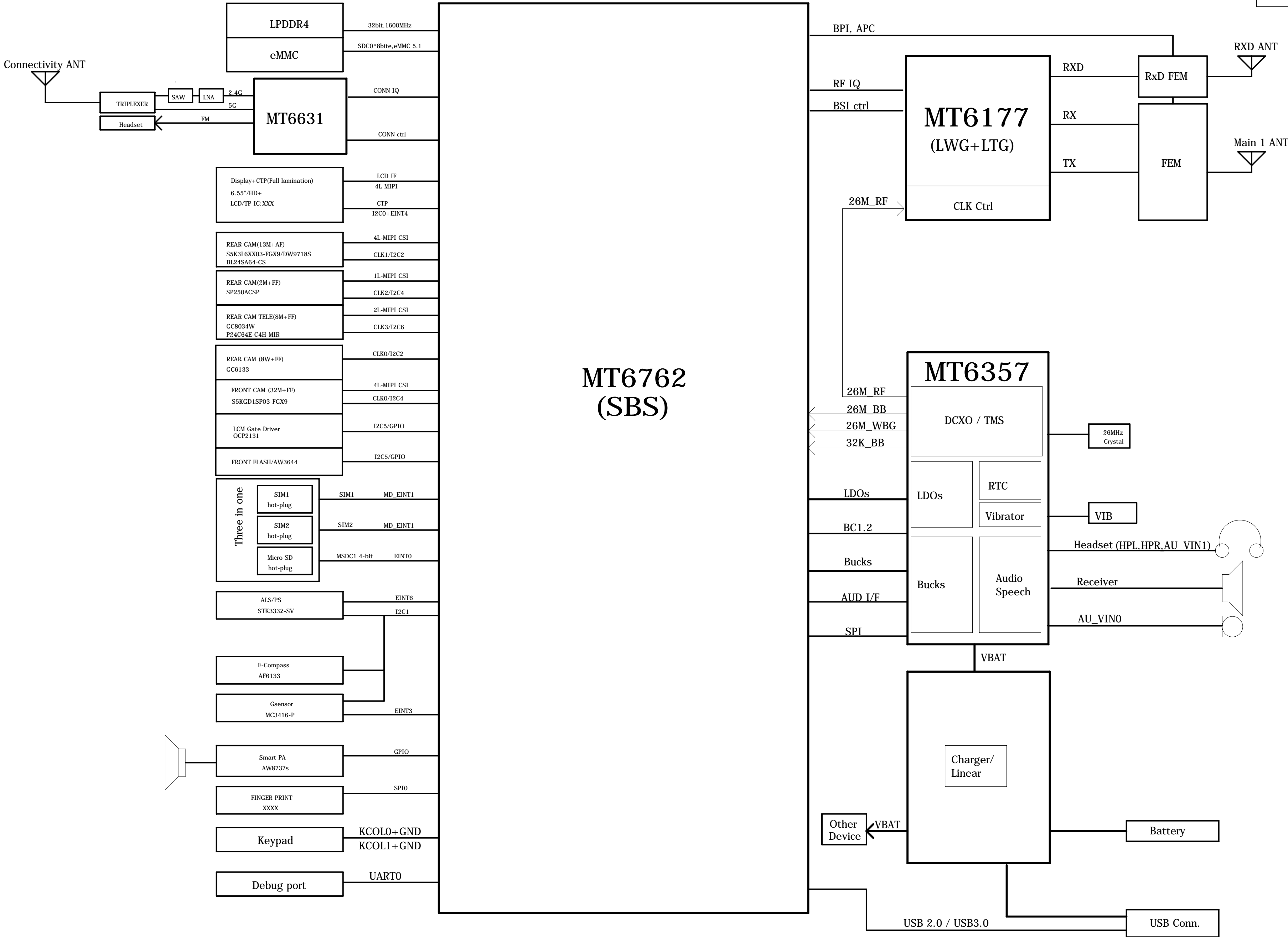


BLOCK_DIAGRAM

Project : MT6762 LPDDR4

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 00_BLOCK_DIAGRAM		VERSION: V1.2	SHEET: 1 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

I2C_ID_OVERVIEW

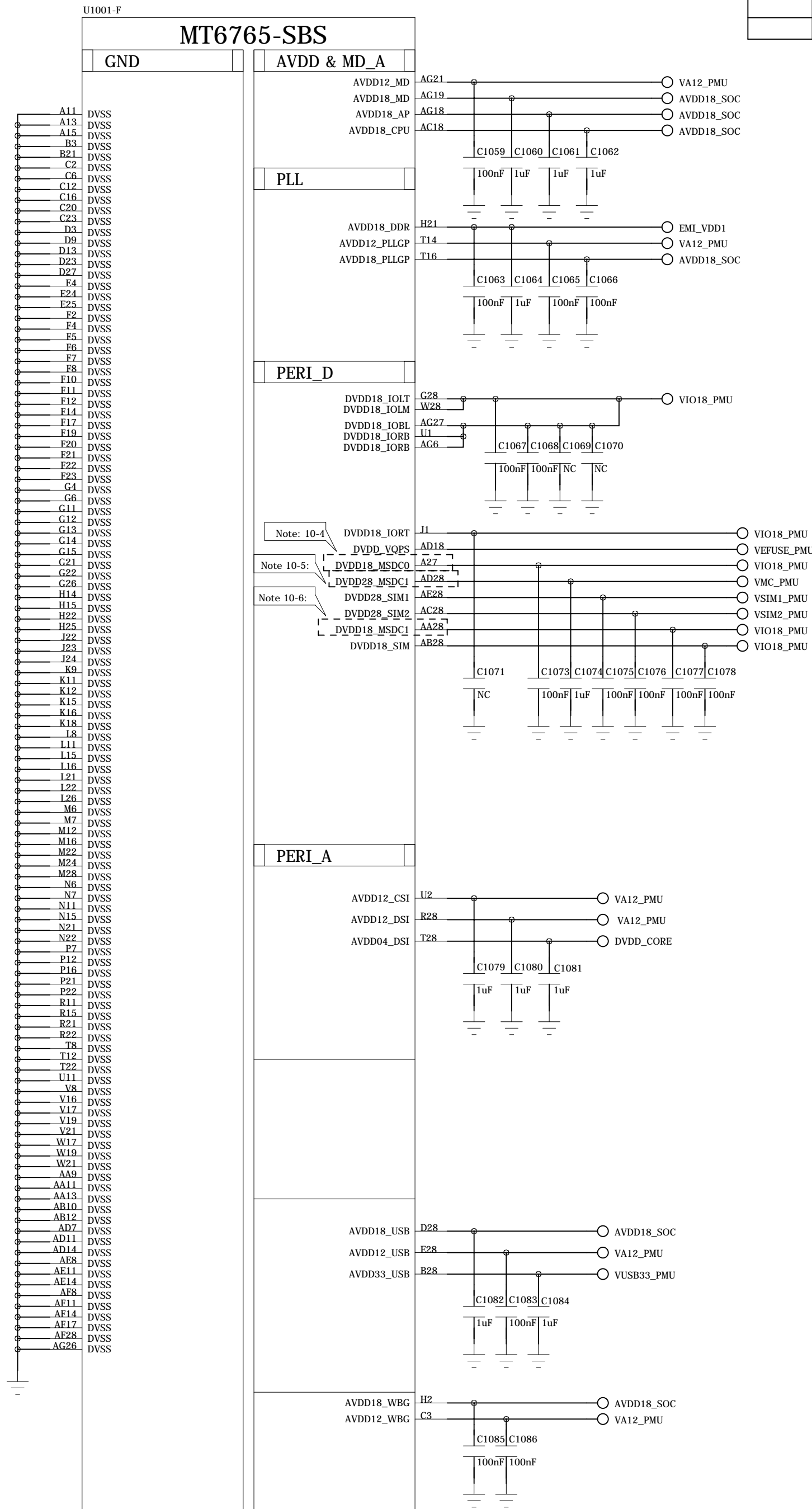
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

I2C	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)
I2C-0	CTP	400 Kbps	Yes.	CTP (NT35672) I2C address: 0X01 (Write:0x02, Read:0x03)
I2C-1	M Sensor	400 Kbps	Yes.	AF6133:I2C ADDRESS:0x18(Write)/0x19(Read)
	ALS / PS Sensor	400 Kbps	Yes.	STK3332-SV address: Write:0xEE, Read:0xEF
	Gsensor	400 Kbps	Yes.	MC3416-P:ADDRESS:0x98(Write)/0x99(Read)
I2C-2	REAR CAMERA Wide (13M+AF)	400 Kbps	Yes.	Back camera(S5K3L6XX03-FGX9) I2C address: (Write:0x20, Read:0x21) EEPROM IC(BL24SA64) I2C address: (Write:0xA2, Read:0xA3) MOTOR IC(DW9718S) I2C address: (Write:0x18, Read:0x19)
	REAR 4 CAMERA	400 Kbps	Yes.	Back camera(GC6133) I2C address: (Write:0x80, Read:0x81)
I2C-3	HL7593WL02	400 Kbps	Yes.	I2C address: 0X57 (Write:0xAE, Read:0xAF)
I2C-4	REAR CAMERA MONO (2M+FF)	400 Kbps	Yes.	Back camera(SP250ACSP) I2C address: (Write:0x78, Read:0x79)
	FRONT CAMERA (32M+FF)	400 Kbps	Yes.	Front camera(S5KGD1SP03-FGX9)I2C address: (Write:0x5A, Read:0x5B) EEPROM IC(P24C64E-C4H-MIR) I2C address: (Write:0xA2, Read:0xA3)
I2C-5				
	LCM Gate Driver	400 Kbps	Yes.	OCP2131:I2C ADDRESS:0x7C(Write)/0x7D(Read)
	Flash Driver	400 Kbps	Yes.	AW3644YFFR:I2C ADDRESS:0xC6(Write)/0xC7(Read)
I2C-6	REAR CAMERA Tele	400 Kbps	Yes.	Back camera(GC8034W) I2C address: (Write:0x6E, Read:0x6F) EEPROM IC(P24C64E-C4H-MIR) I2C address: (Write:0xA0, Read:0xA1)

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

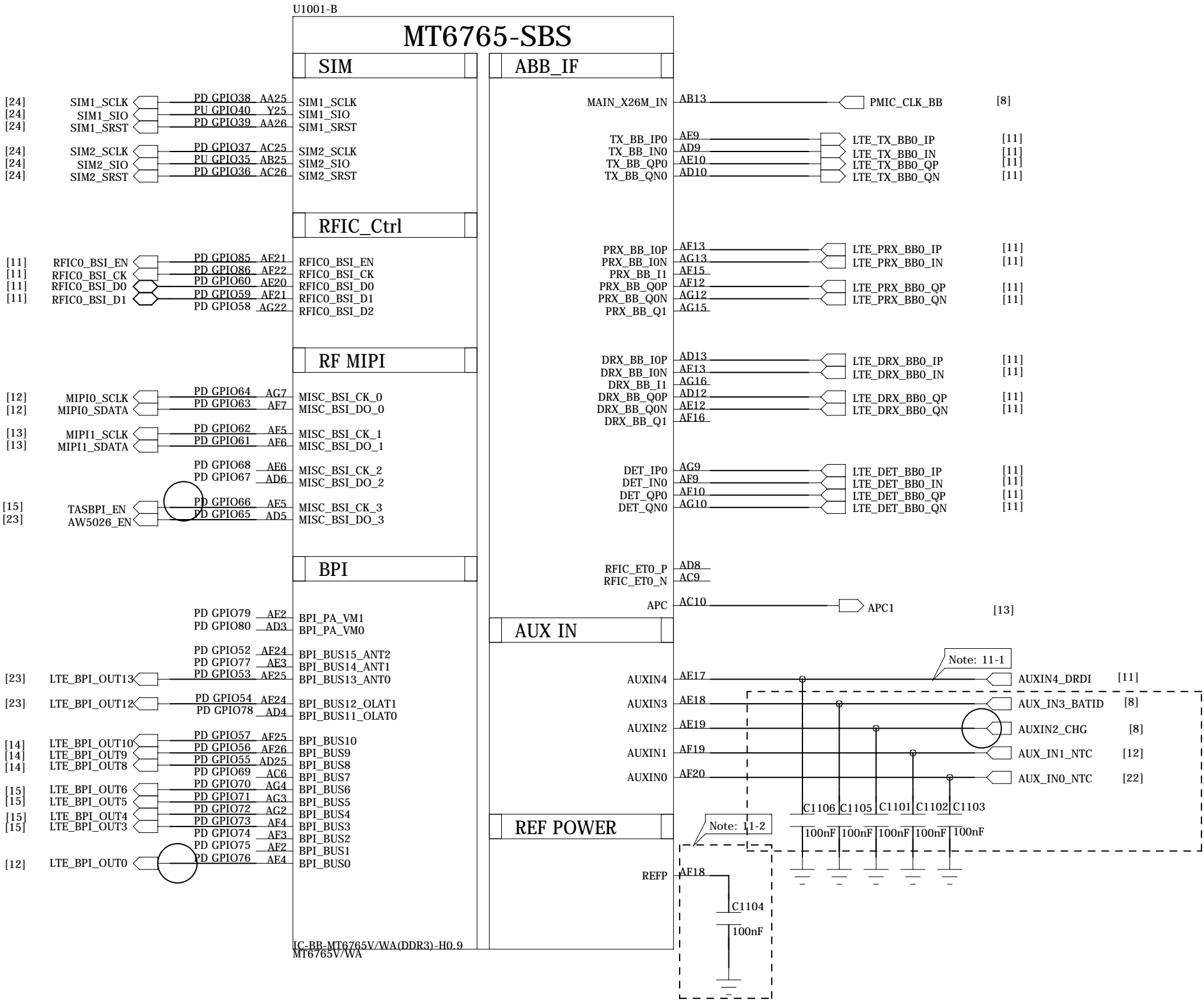
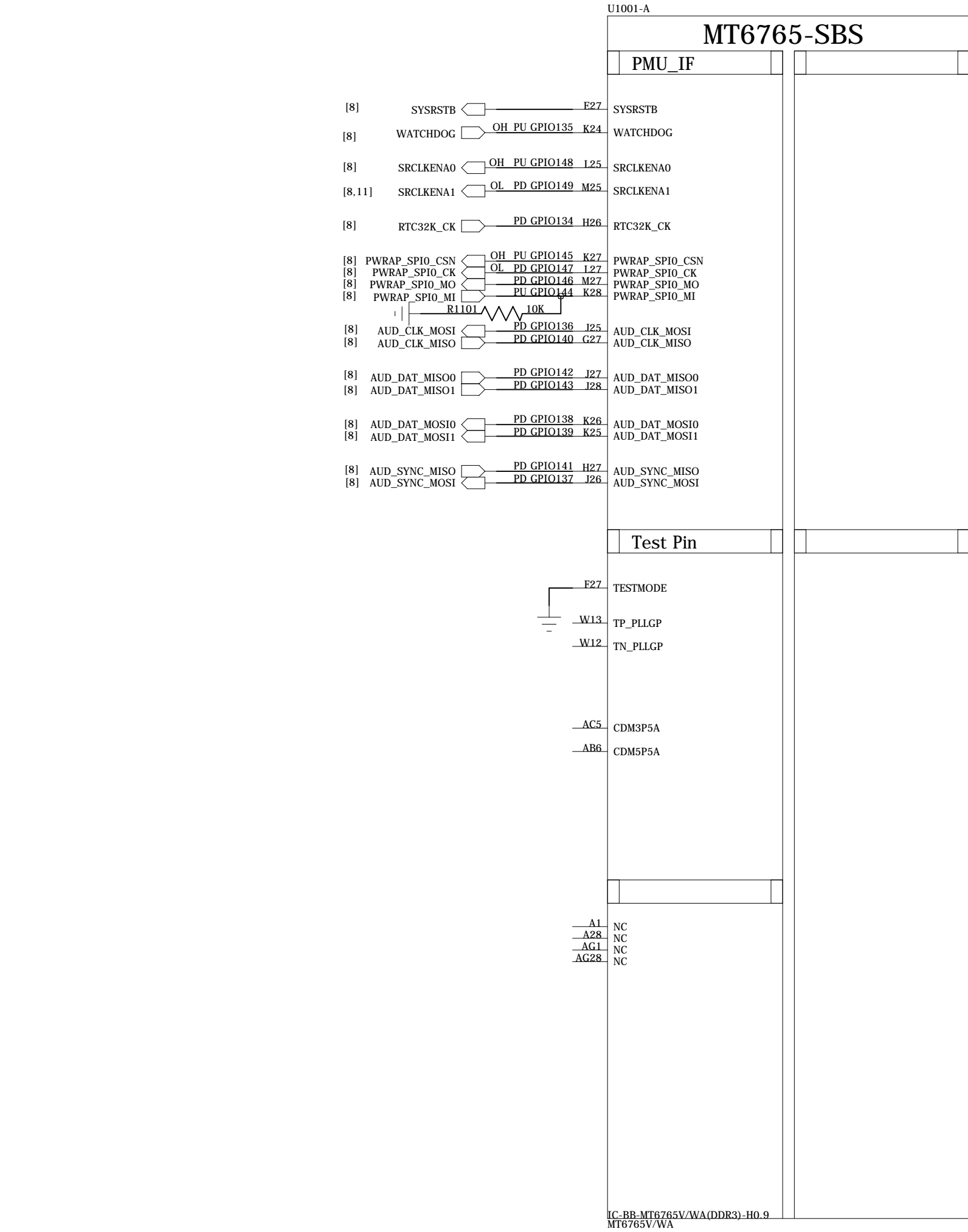
COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 01_I2C_ID_OVERVIEW		VERSION: V1.2	SHEET: 2 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



SHEET: 3 OF 24

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



RFIC_Ctrl

RF MIPI

BPI

MAIN_X26M_IN

TX_BB_IP0

TX_BB_IN0

TX_BB_QP0

TX_BB_QN0

PRX_BB_I0P

PRX_BB_I0N

PRX_BB_I1

PRX_BB_Q0P

PRX_BB_Q0N

PRX_BB_Q1

DRX_BB_I0P

DRX_BB_I0N

DRX_BB_I1

DRX_BB_Q0P

DRX_BB_Q0N

DET_IP0

DET_IN0

DET_QP0

DET_QN0

RFIC_ET0_P

RFIC_ET0_N

APC

AUXIN4

AUXIN3

AUXIN2

AUXIN1

AUXIN0

REFP

PMIC_CLK_BB

LTE_TX_BBO_IP

LTE_TX_BBO_IN

LTE_TX_BBO_QP

LTE_TX_BBO_QN

LTE_PRX_BBO_IP

LTE_PRX_BBO_IN

LTE_PRX_BBO_QP

LTE_PRX_BBO_QN

LTE_DRX_BBO_IP

LTE_DRX_BBO_IN

LTE_DRX_BBO_QP

LTE_DRX_BBO_QN

LTE_DET_BBO_IP

LTE_DET_BBO_IN

LTE_DET_BBO_QP

LTE_DET_BBO_QN

APC1

AUXIN4_DRD1

AUX_IN3_BATID

AUXIN2_CHG

AUX_IN1_NTC

AUX_IN0_NTC

C1104

IC-BB-MT6765V/WA(DDR3)-H0.9
MT6765V/WA

"PWRAP_SPI0_CSN" and "AUD_DAT_MOSIO" are bootstrap pin to slect which interface will be the JTAG pin out.				
	PWRAP_SPI0_CSN	AUD_DAT_MOSIO	AP_JTAG	IO_JTAG
Default	(PU) HI	(PD) LO	N/A	N/A
	HI	HI (by req. P0)	SPI_CSB/SPI_CLK/SPI_MO/SPI_MI/EINT8	N/A
	LO (by req. P0)	LO	SPI_CSB/SPI_CLK/SPI_MO/SPI_MI/EINT8	SPI1+SPI3
	LO (by req. P0)	HI (by req. P0)	MSDC1_CLK/CMD/DAT0/DAT1/DAT2	N/A

Note 22-4: PWRAP_SPI0_MI are DDR type feature in bootstrap			
	PWRAP_SPI0_MI	Bootting interface	
	Default=PU	DDR	MSDC0 pin mux
	LO (by req. P0)	LPDDR3	follow LP3 Ref SCH.
Default	HI	LPDDR4X	follow LP4X Ref SCH.

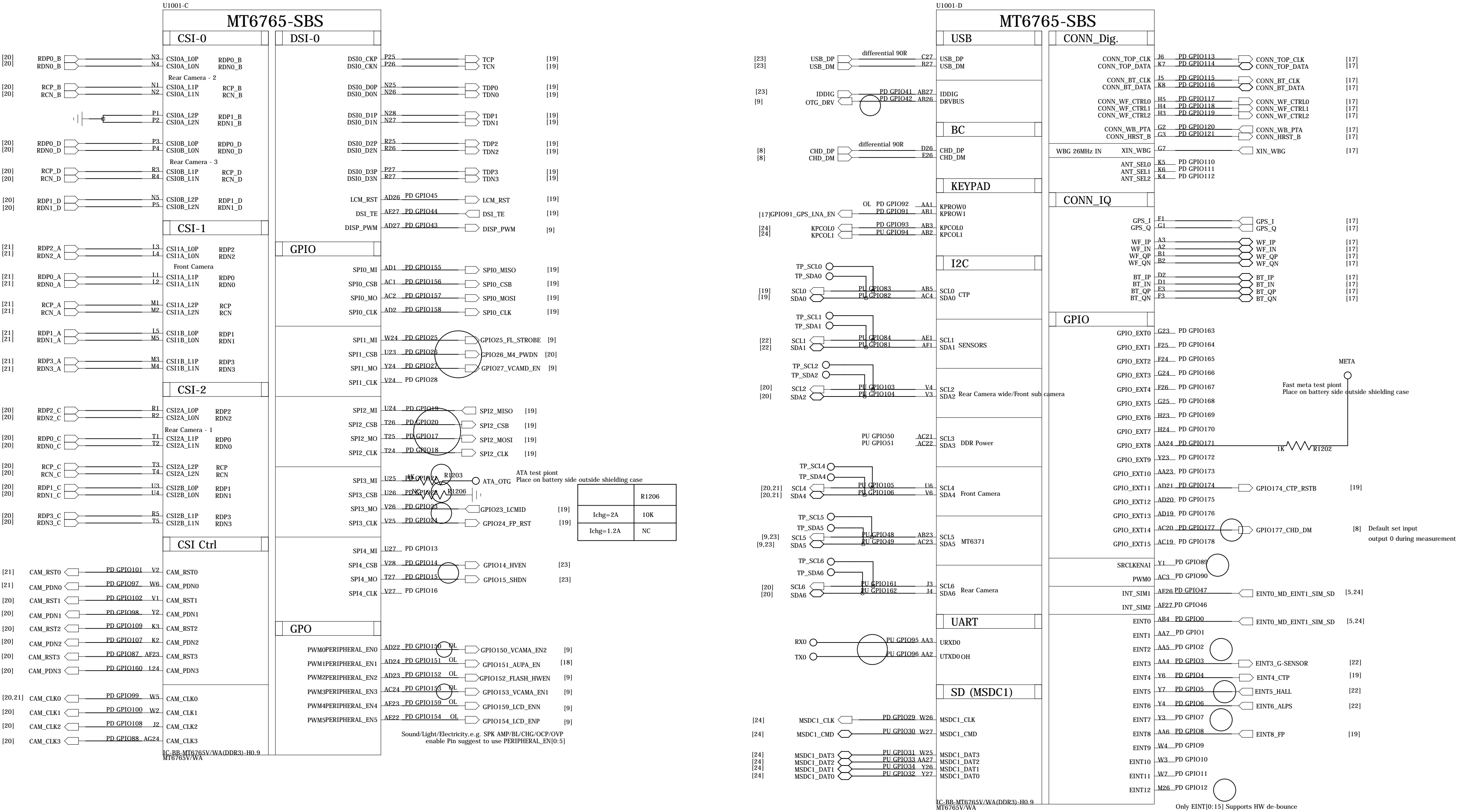
COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 11_BB_I		VERSION: V1.2	SHEET: 4 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

Schematic design notice of "11_BB_I" page.

Note 11-1: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 11-2: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



IC: BB-MT6765V/WA(DDR3)-H0.9

MT6765V/WA

IC: BB-MT6765V/WA(DDR3)-H0.9

MT6765V/WA

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

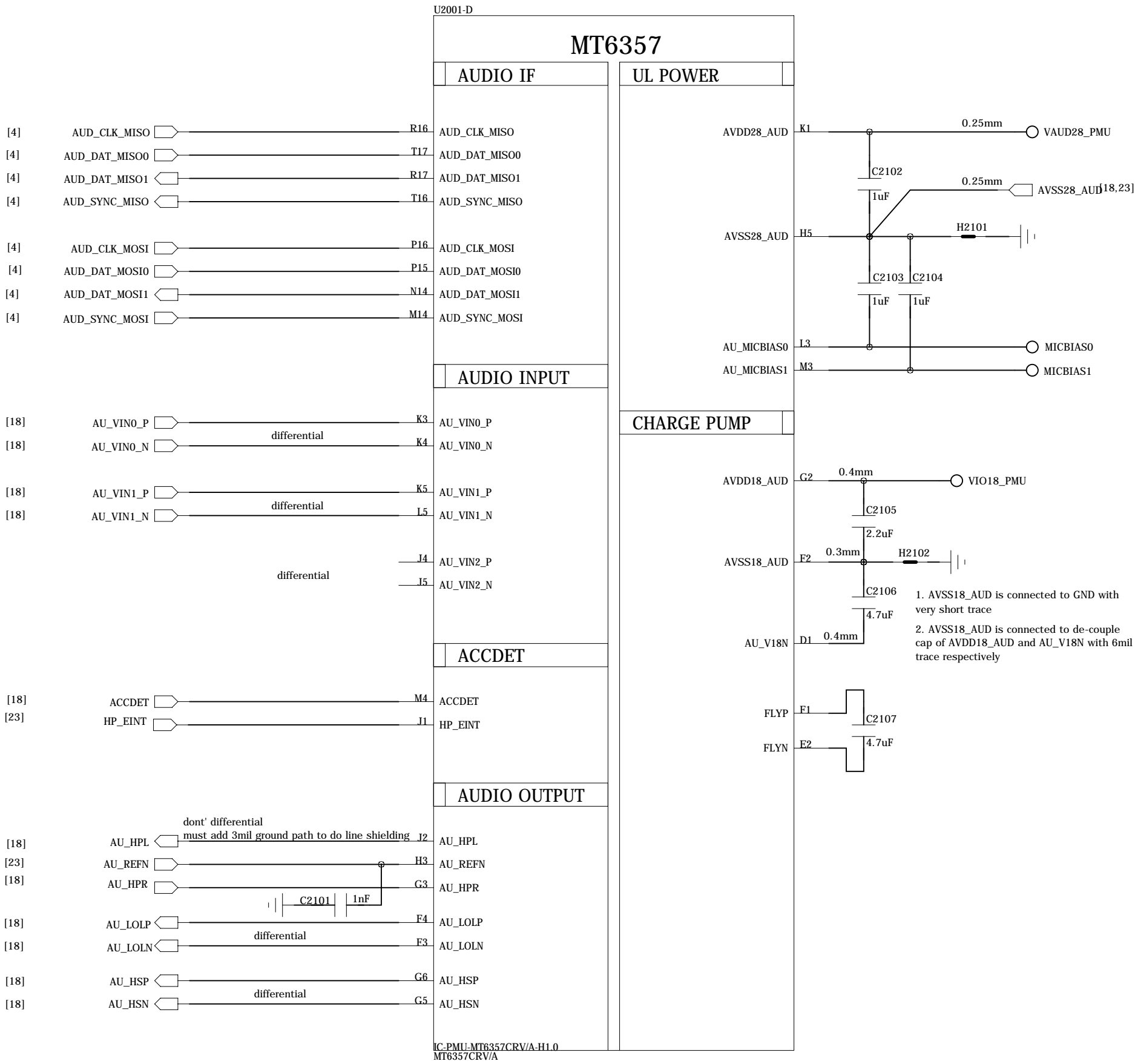
[illegible]

COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 20_POWER_MT6357_I		VERSION: V1.2	SHEET: 7 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

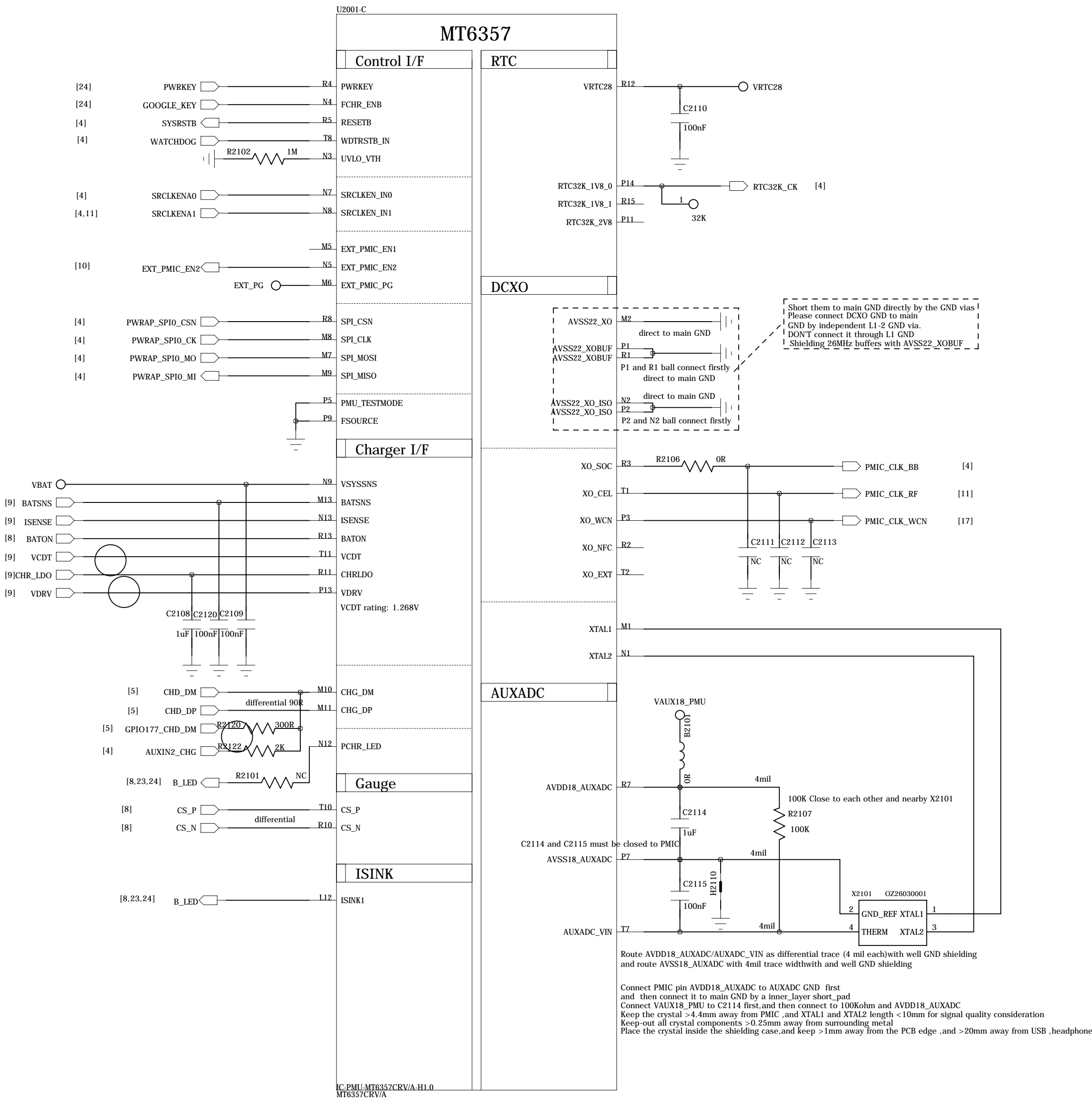
POWER_MT6357_II

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

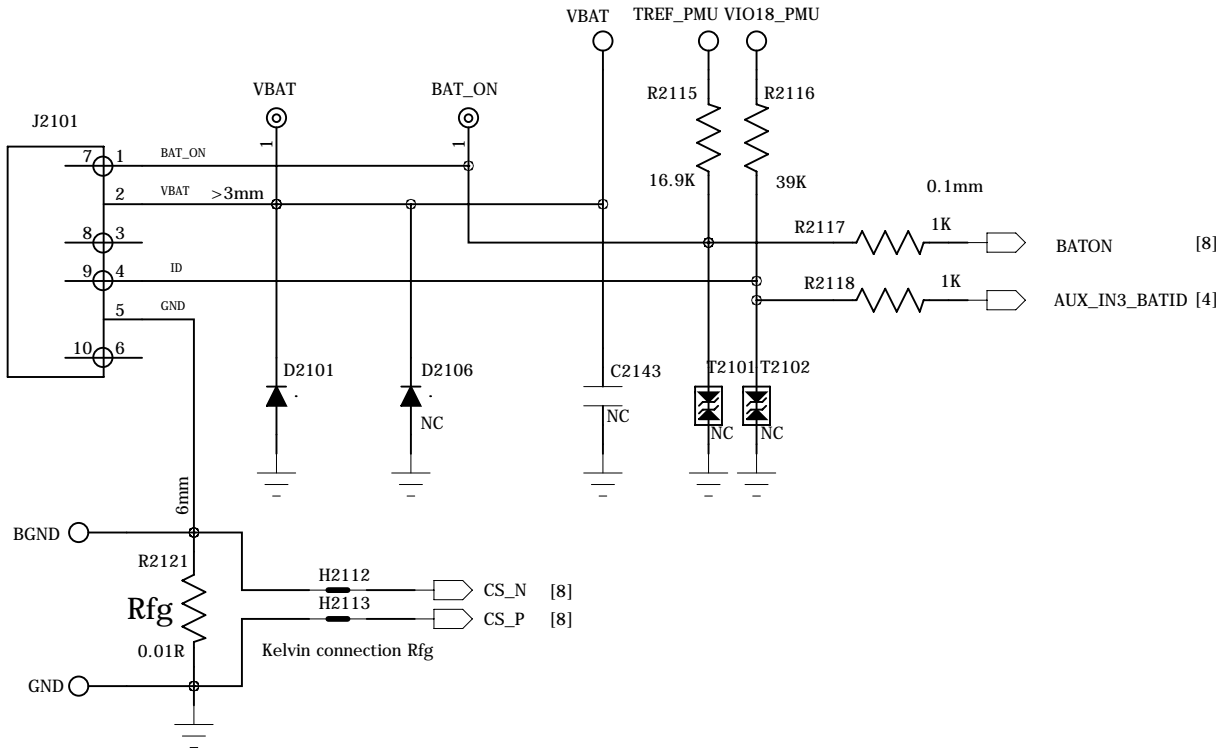
PMU_AUDIO



PMU_CLK



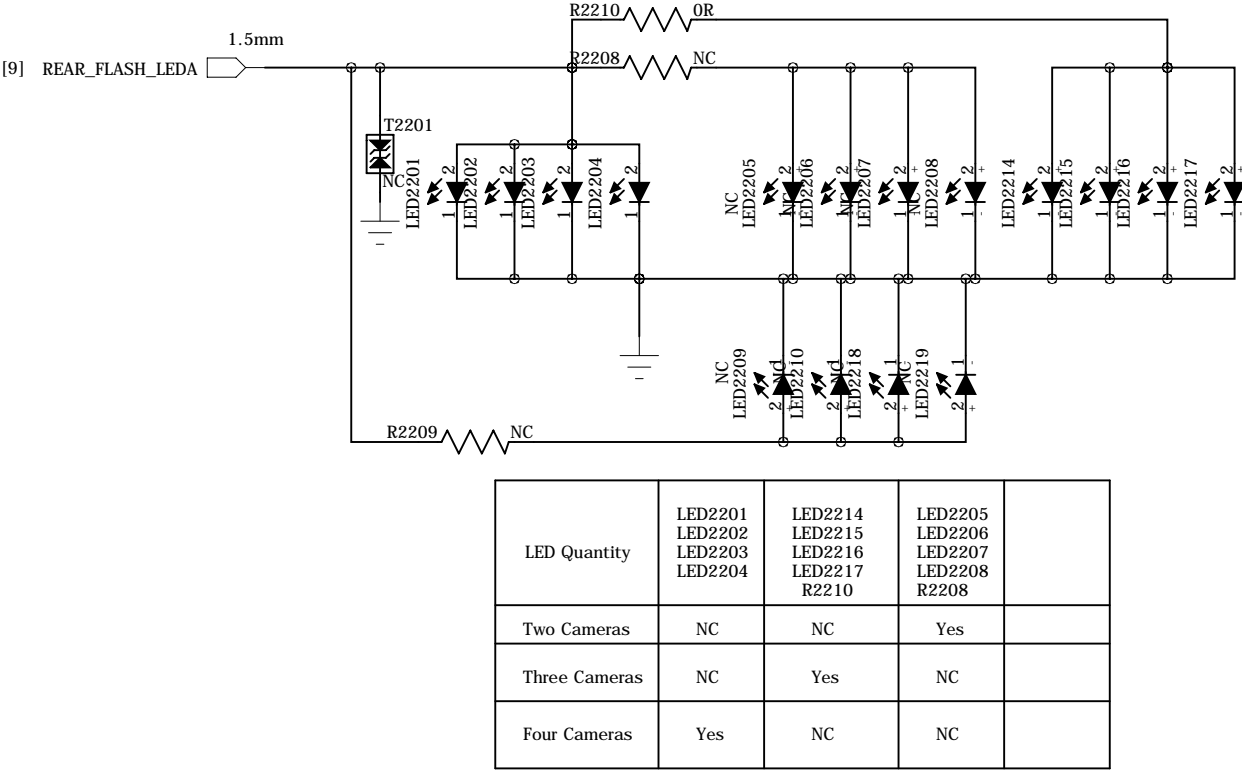
BATTERY CONNECTOR



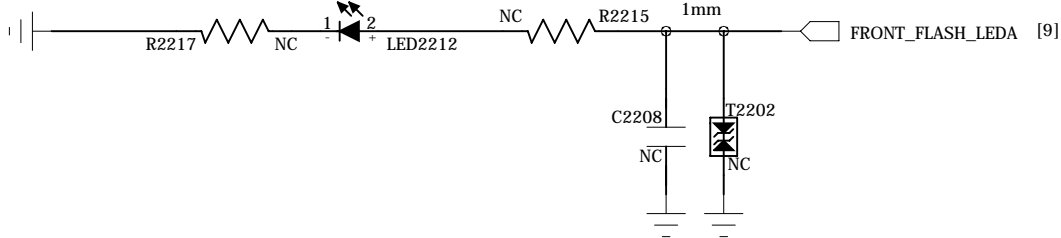
COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 21_POWER_MT6357_II		VERSION: V1.2	SHEET: 8 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

POWER_THIRD-PARTY_I

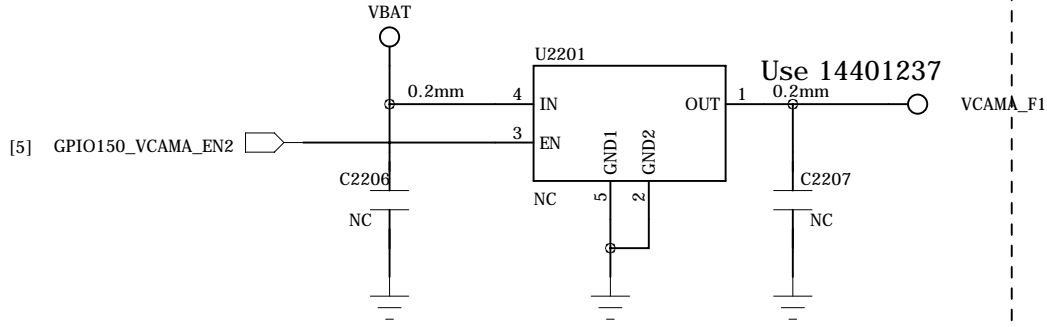
Rear Flash LED



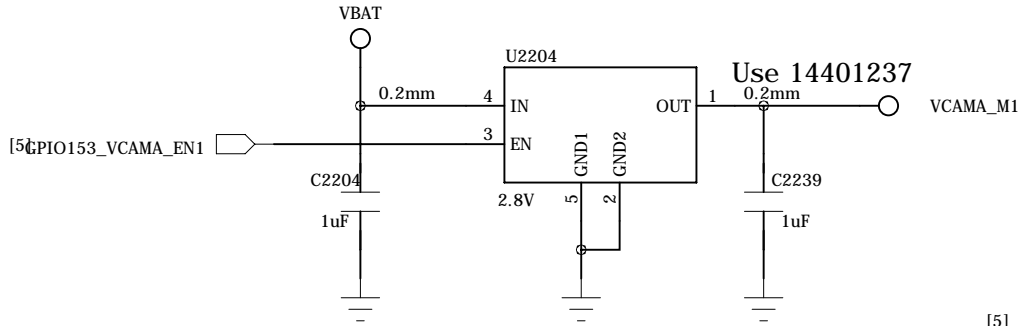
Front Flash LED



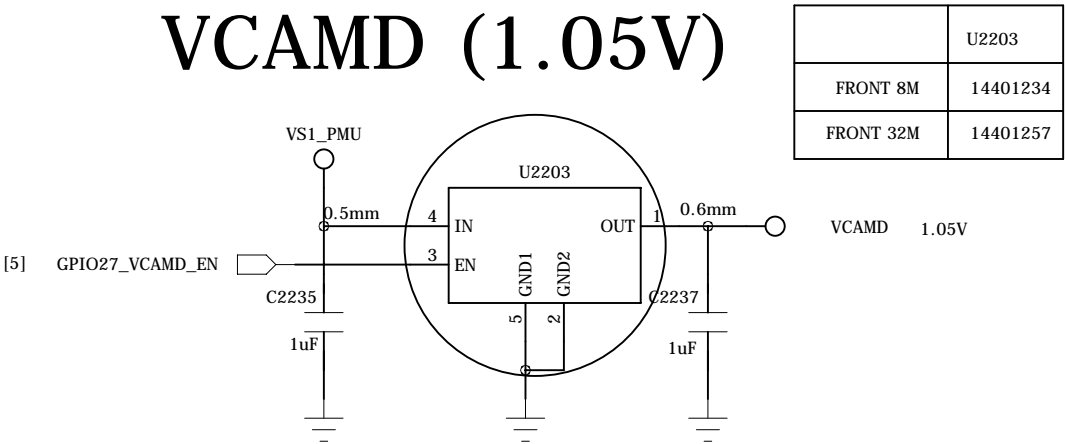
VCAMA_F1(2.8V)



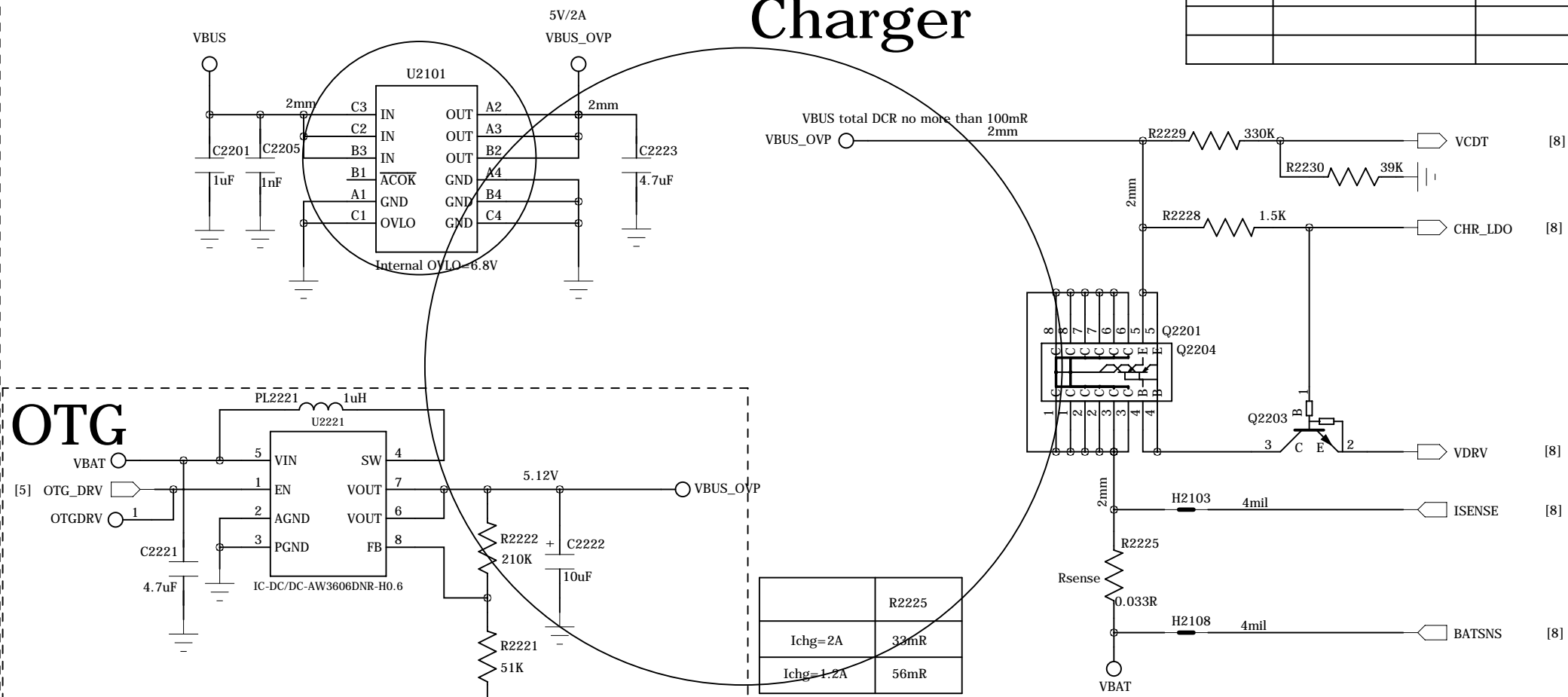
VCAMA_M1(2.8V)



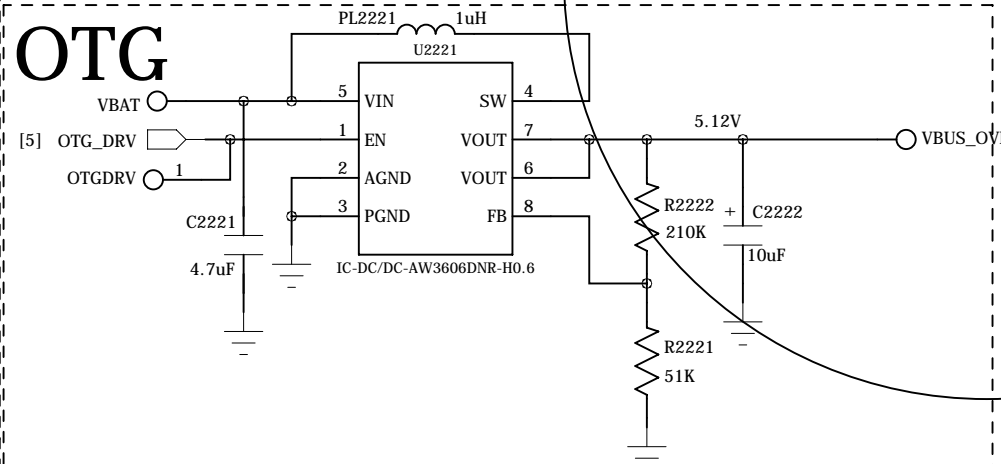
VCAMD (1.05V)



Charger

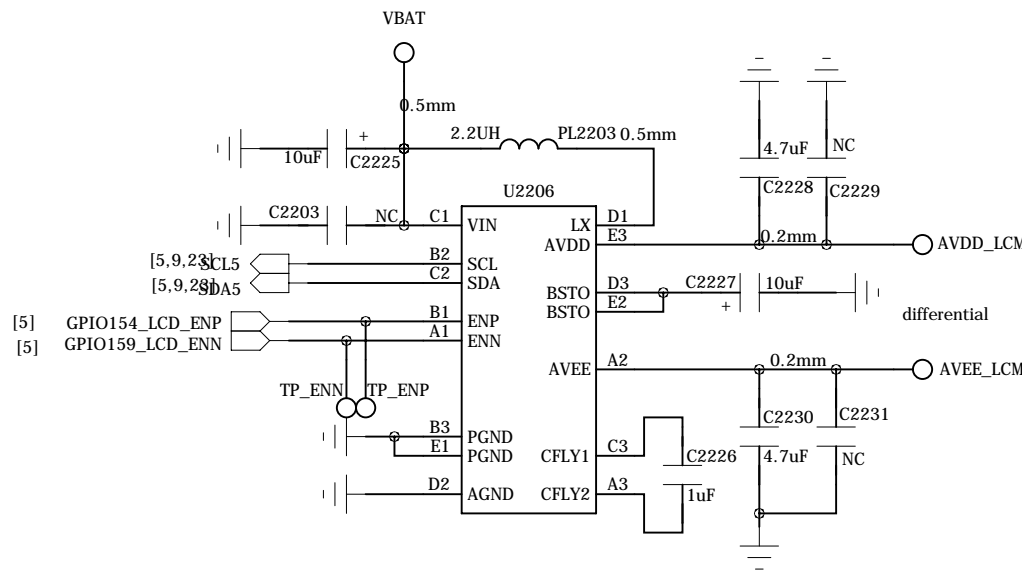


OTG



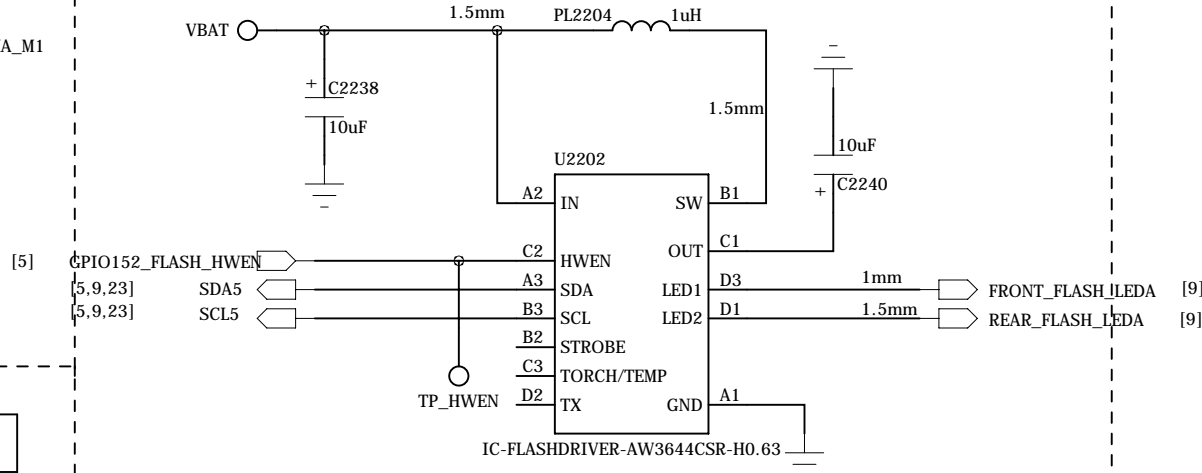
LCD--BIAS

0CP2131:12C ADDRESS:0x7C(Write)/0x7D(Read)

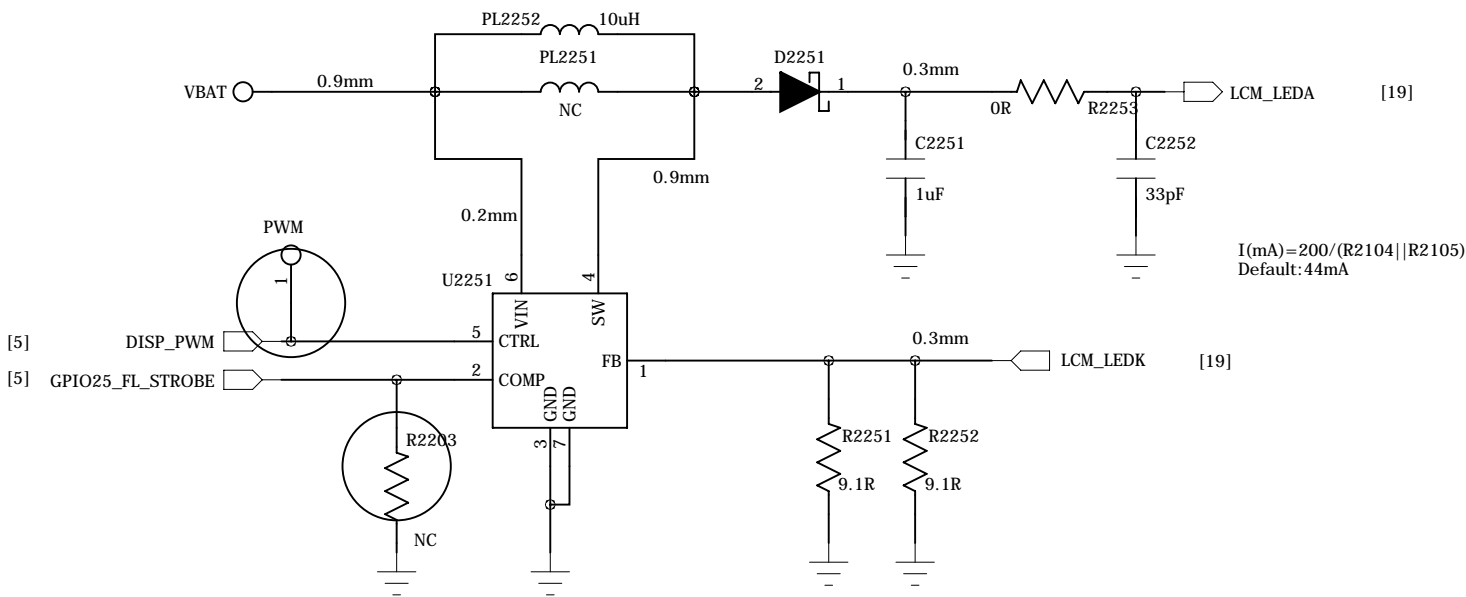


Flash Driver

AW3644YFFR:12C ADDRESS:0xC6(Write)/0xC7(Read)



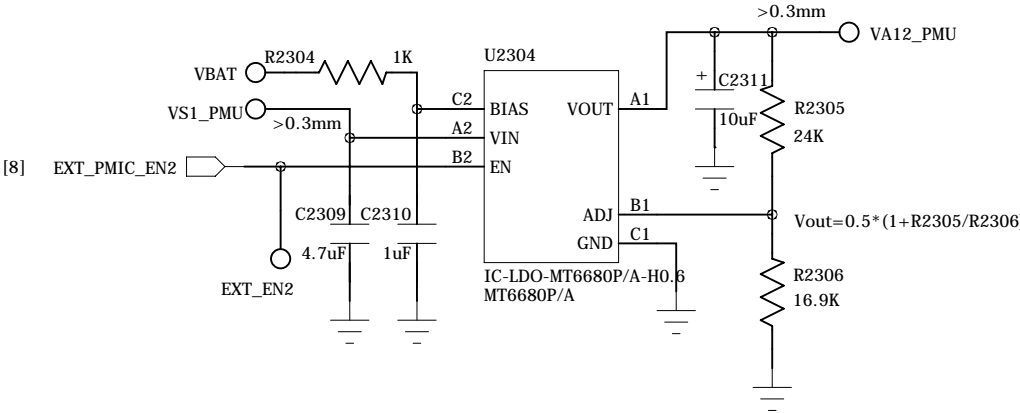
Backlight and face flash



COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 22_POWER_THIRD-PARTY_I		VERSION: V1.2	SHEET: 9 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

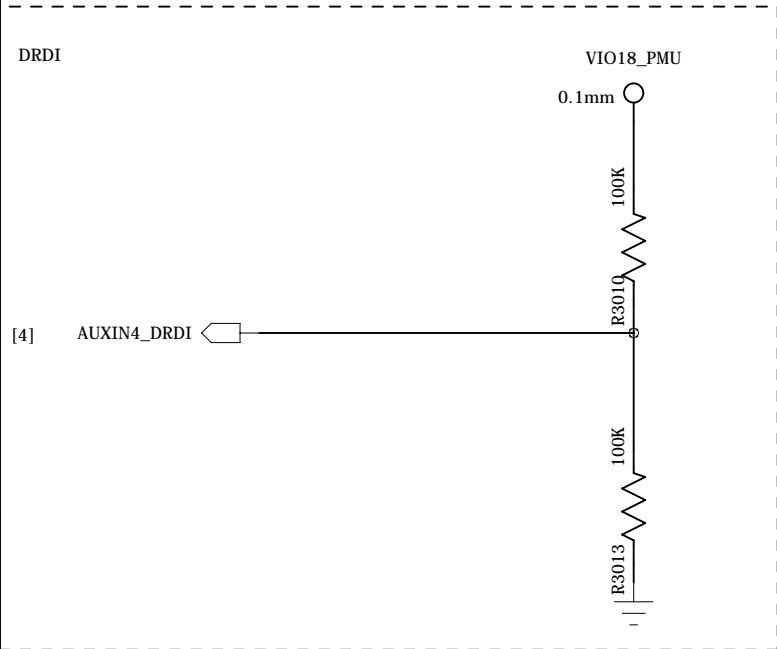
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

LDO 1.2V for VA12



COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 23_POWER_THIRD-PARTY_II		VERSION: V1.2	SHEET: 10 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



VIO18_PMU 0.2mm VIO18_PMU

VRF18_PMU 0.4mm VRF18_PMU

VRF12_PMU 0.25mm VRF12_PMU

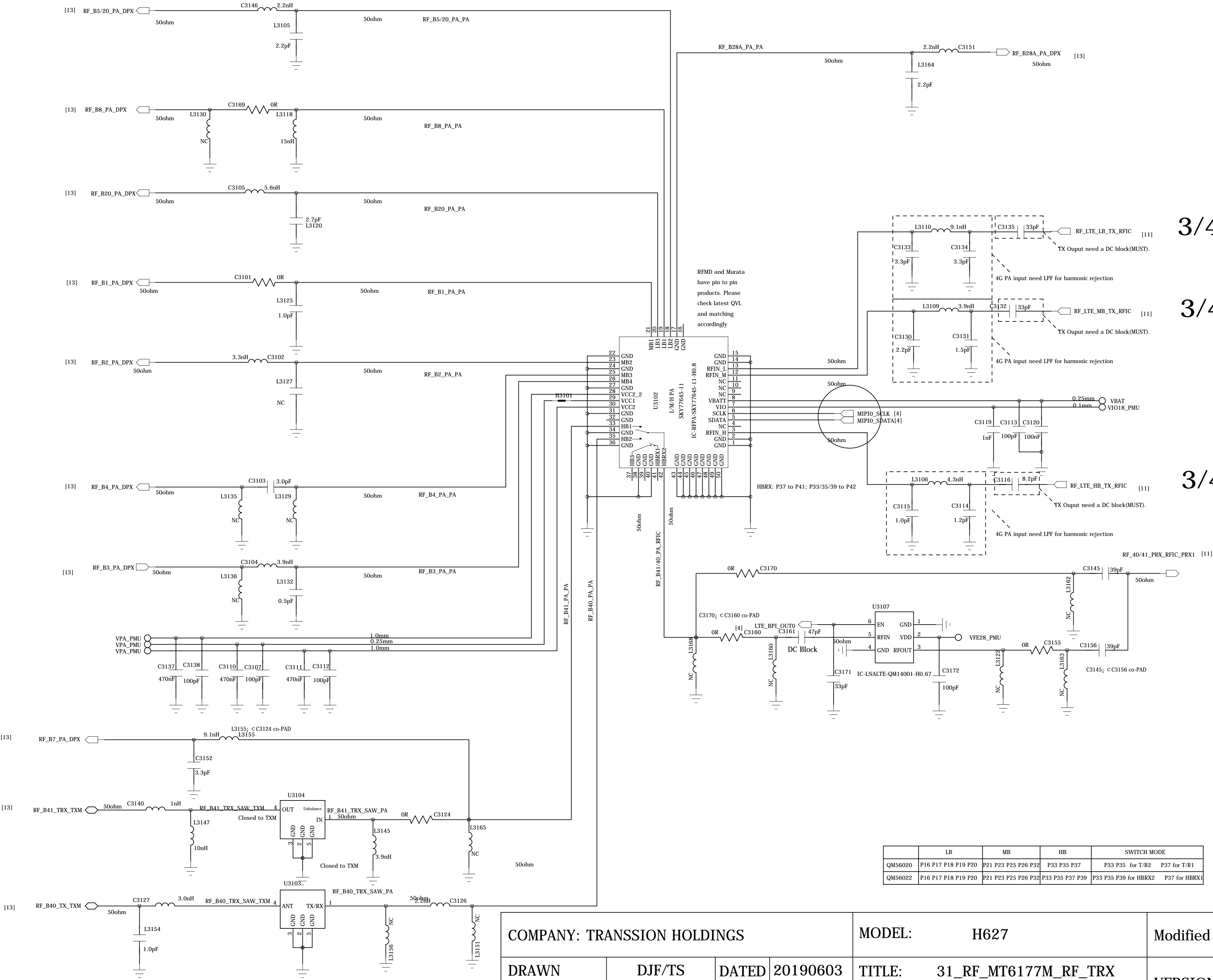
C3007 4.7uF

C3008 4.7uF

COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 30_RF_MT6177M_PIN_OUT		VERSION: V1.2	SHEET: 11 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

RF_MT6176_RF_TX

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



3/4G_PAIN_LB

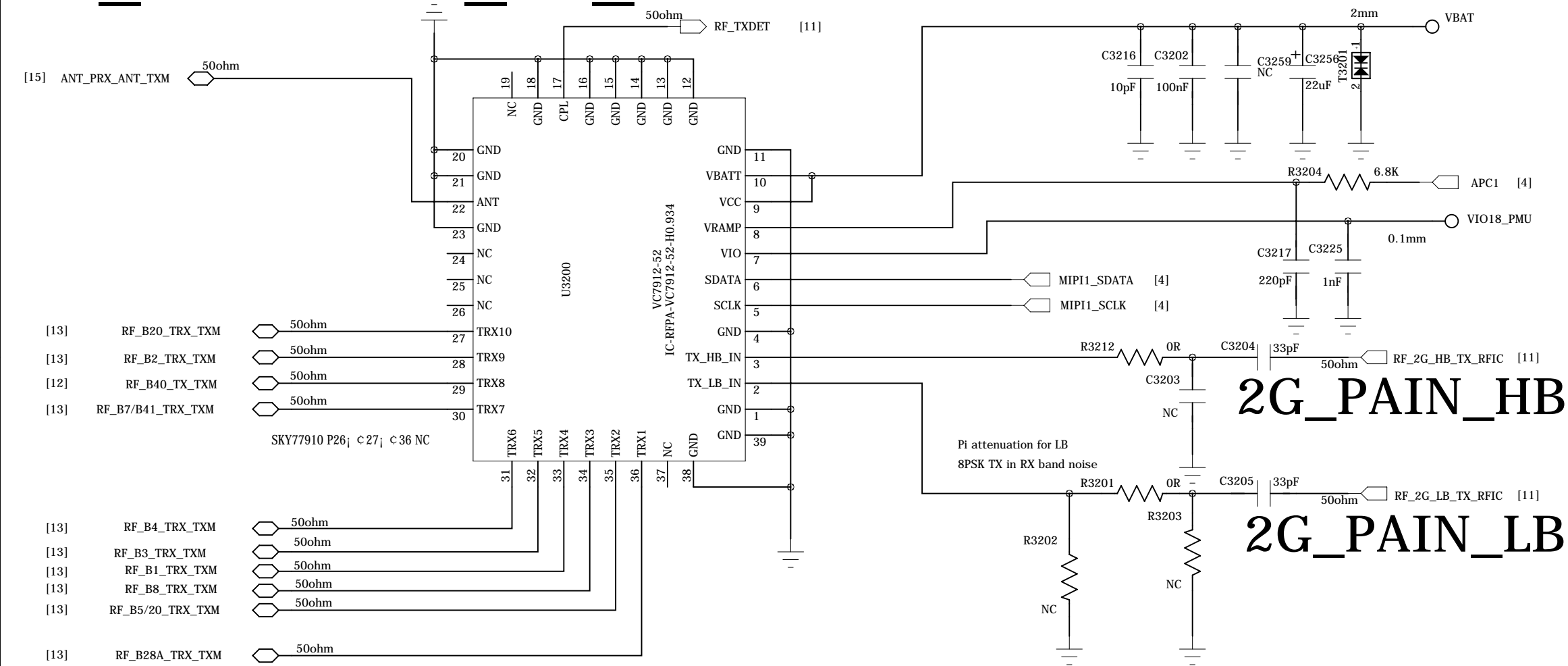
3/4G_PAIN_MB

3/4G_PAIN_HB

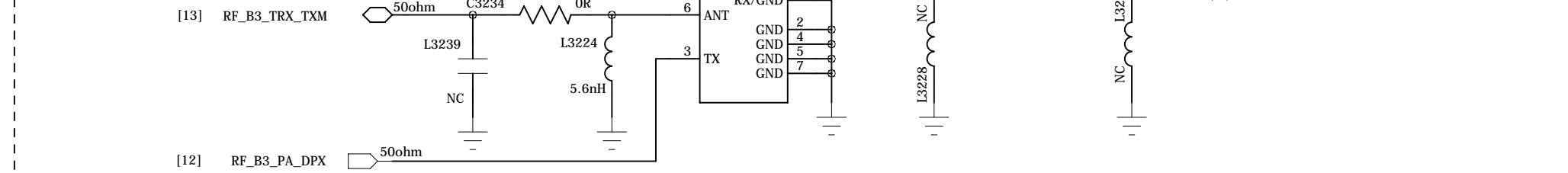
COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 31_RF_MT6177M_RF_TRX		VERSION: V1.2	SHEET: 12 OF 24
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RF_MT6177M_RF_PRX

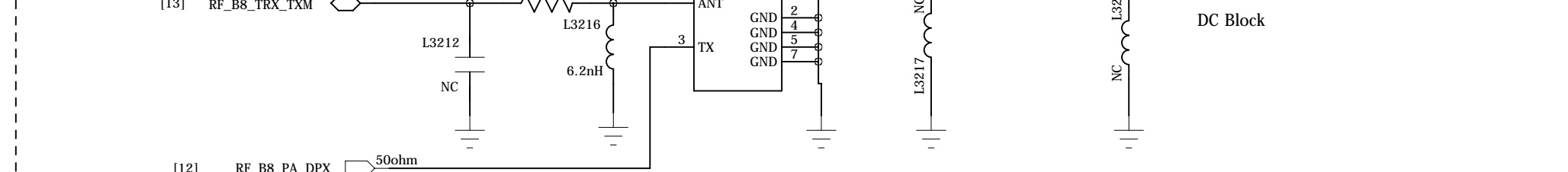
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LTR	ECO NO:	APPROVED:	DATE:



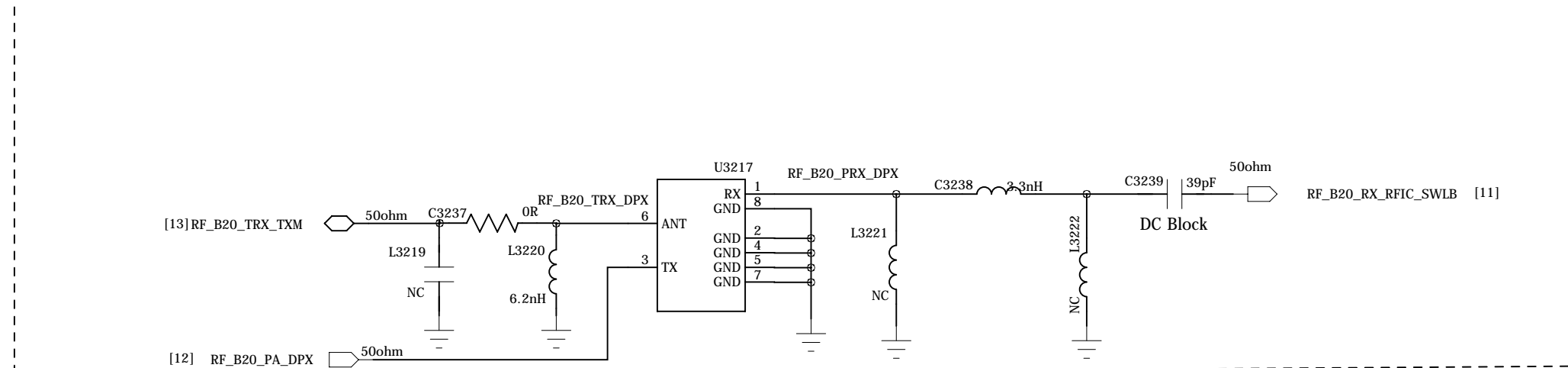
B3_B3_B3



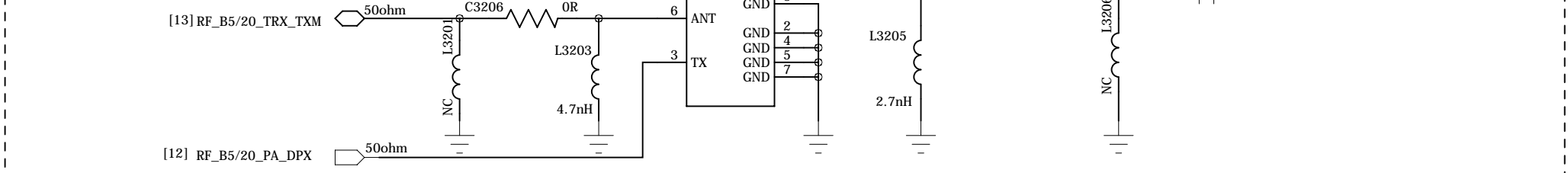
B8_B8_B8



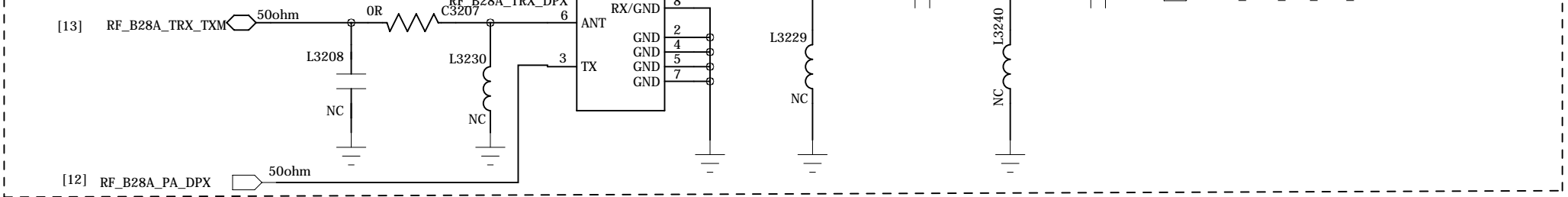
NC_NC_B20



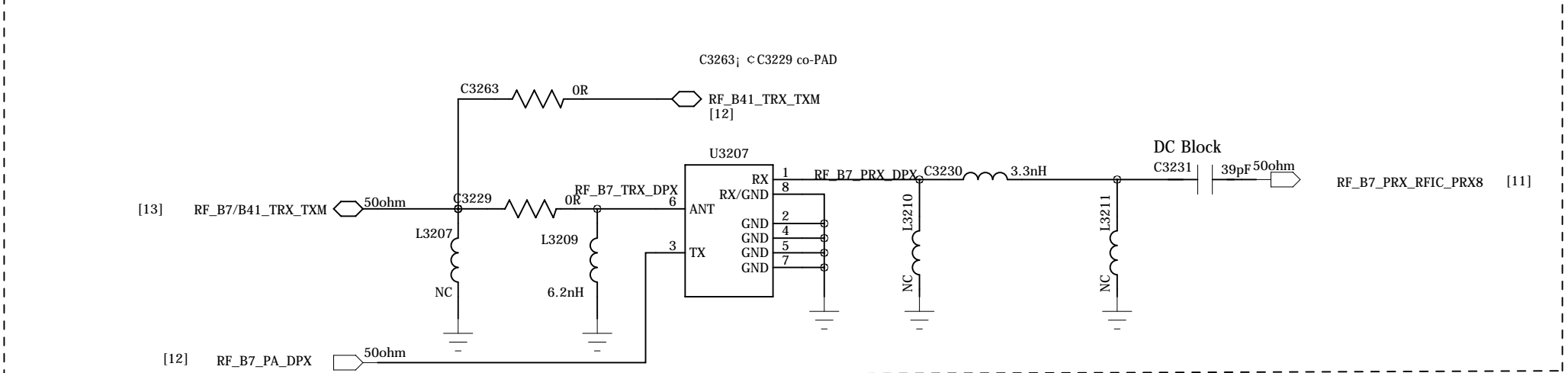
NC_NC_B28A



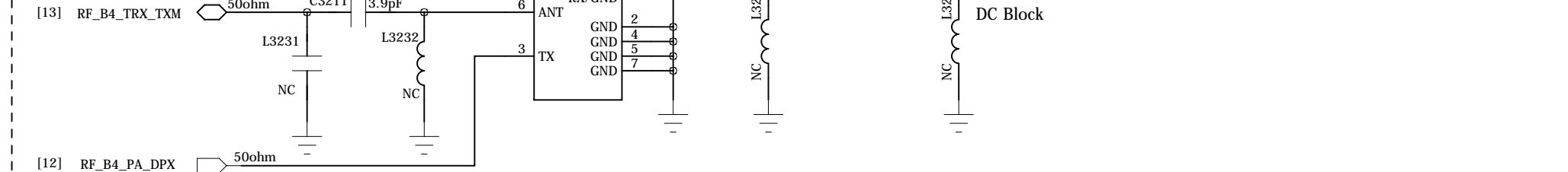
B20_B5_B5



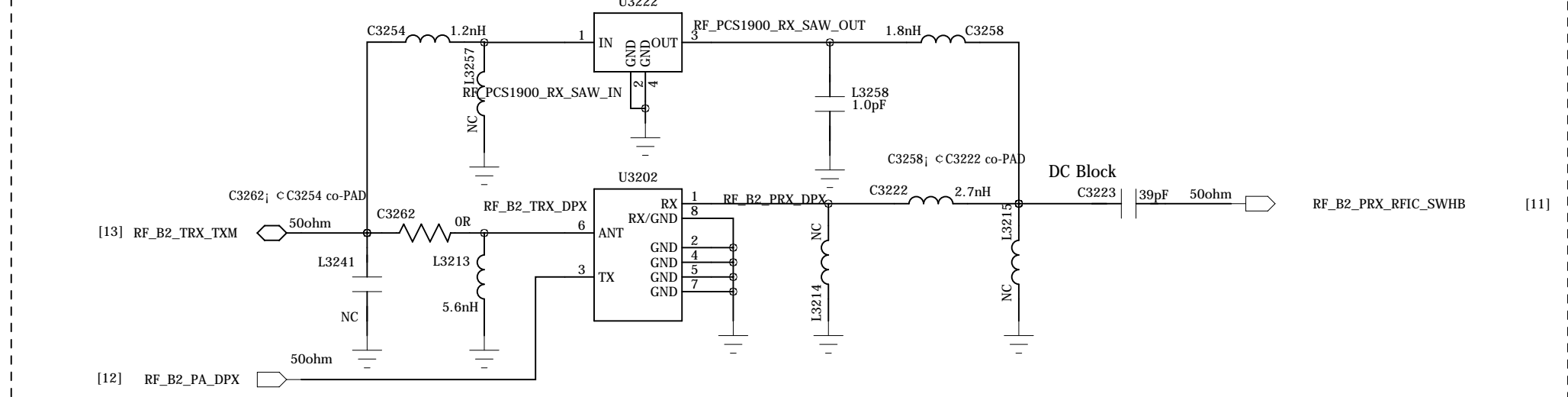
B7_B41_B7



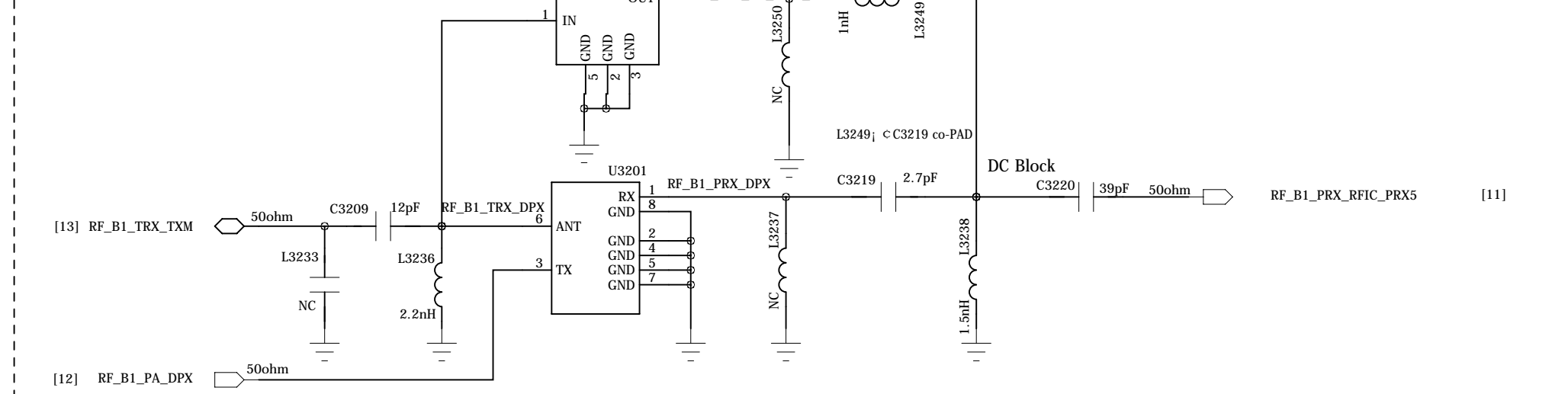
B1_B1_B1



NC_2GHBRX_B2



NC_B40RX_B4



Notice:
NC_PCS_B2_2GHBRX:Africa Bom NC;India Bom PCS;South America BOM B2;3G 2GHBRX;

COMPANY: TRANSSION HOLDINGS

MODEL: H627

Modified Date: 2019/7/4

DRAWN

DJF/TS

DATED

20190603

TITLE:

32_RF_MT6177M_RF_PRX

VERSION: V1.2

SHEET: 13 OF 24

CHECKED

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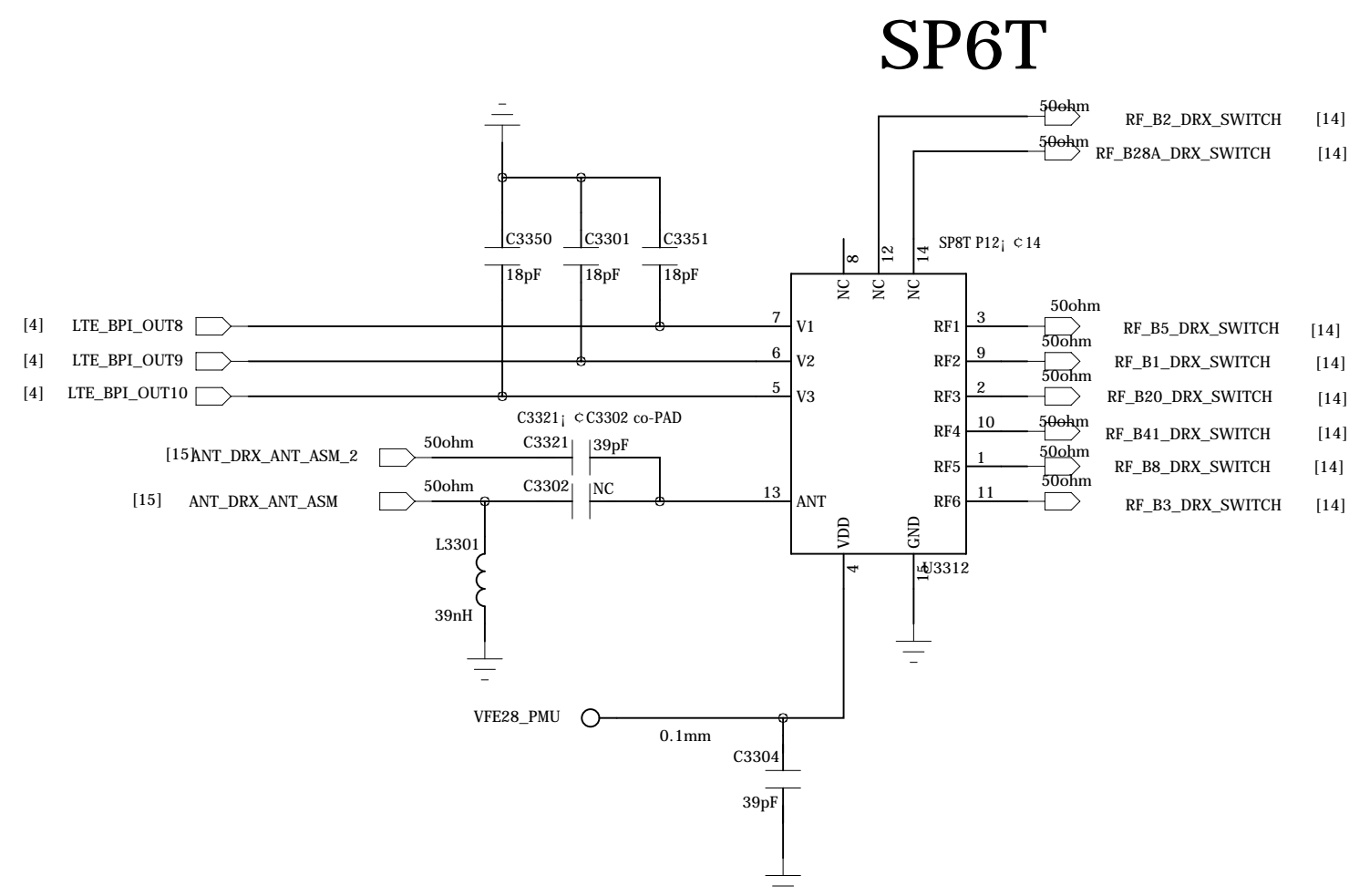
DATED

< >

Confidentiality

CONFIDENTIAL

RF_MT6177M_RF_DRX



SP8T control logic										
SP6T control logic										
V1	V2	V3	RF1	RF2	RF3	RF4	RF5	RF6	RF7	RF8
L	L	L	Y	N	N	N	N	N	N	N
L	L	H	N	Y	N	N	N	N	N	N
L	H	L	N	N	Y	N	N	N	N	N
L	H	H	N	N	N	Y	N	N	N	N
H	L	L	N	N	N	N	Y	N	N	N
H	L	H	N	N	N	N	N	Y	N	N
H	H	L	N	N	N	N	N	N	Y	N
H	H	H	N	N	N	N	N	N	N	Y

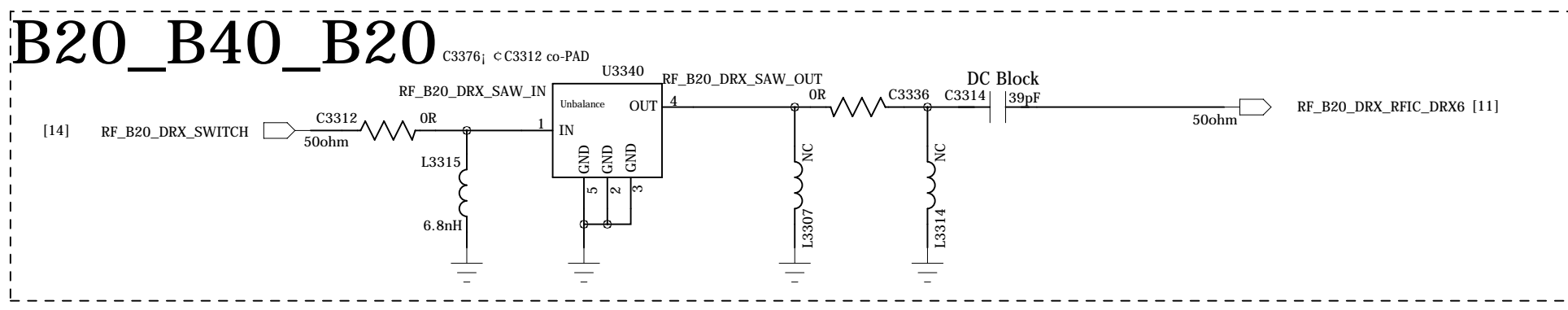
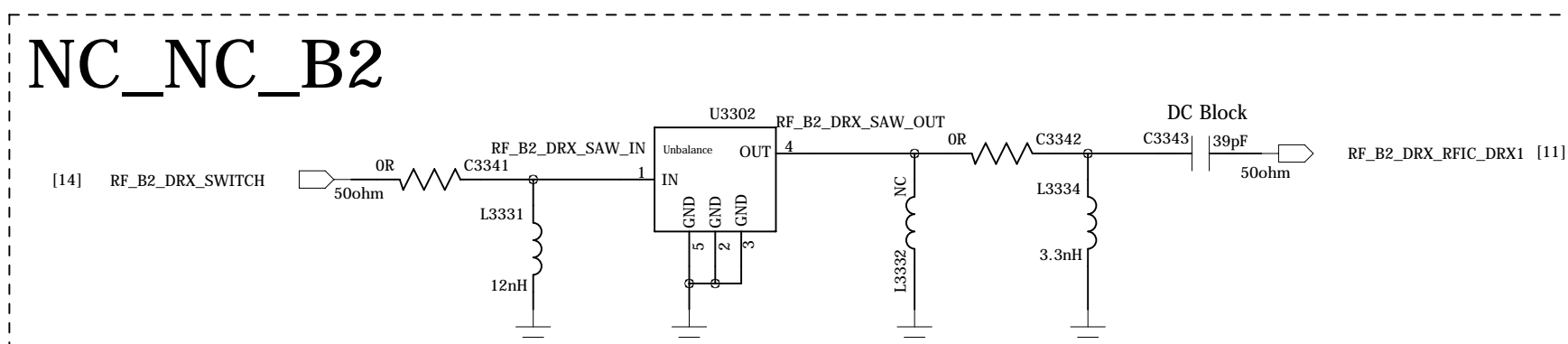
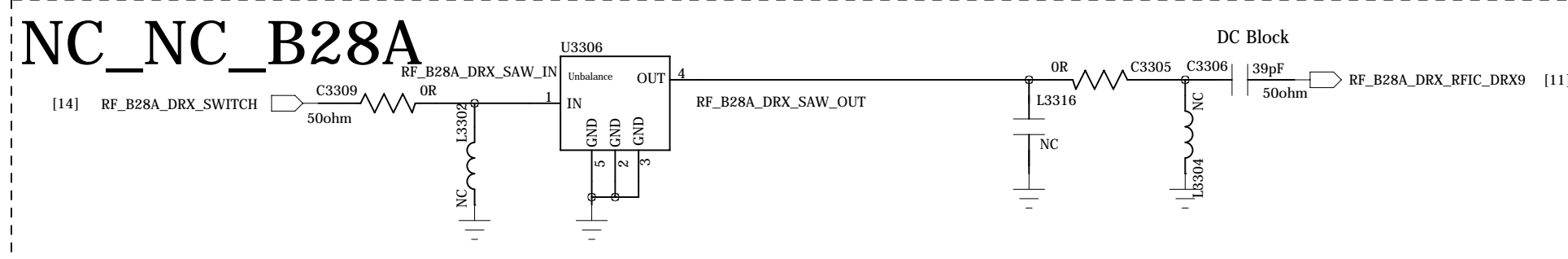
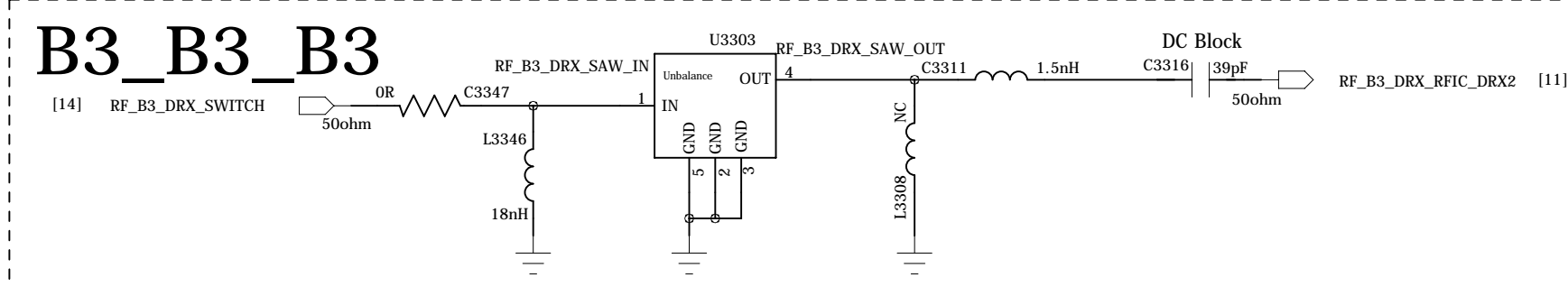
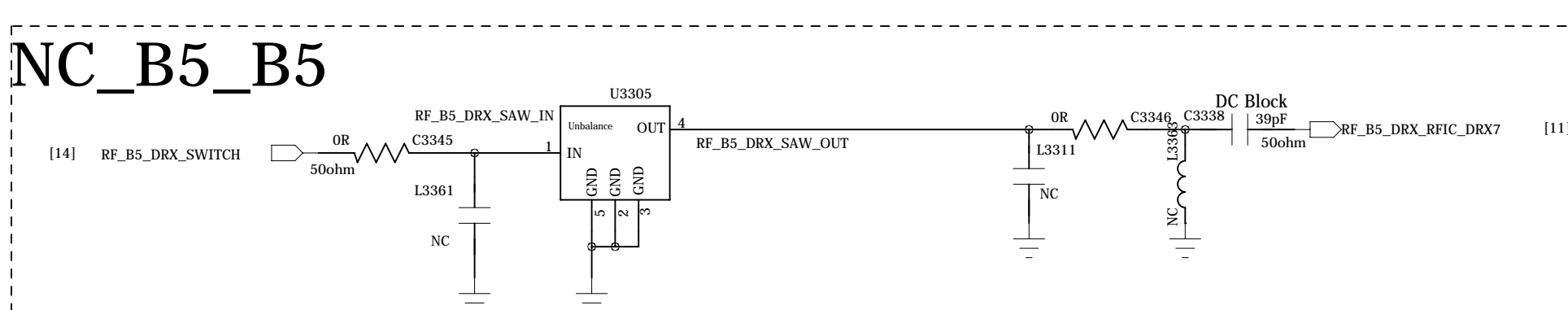
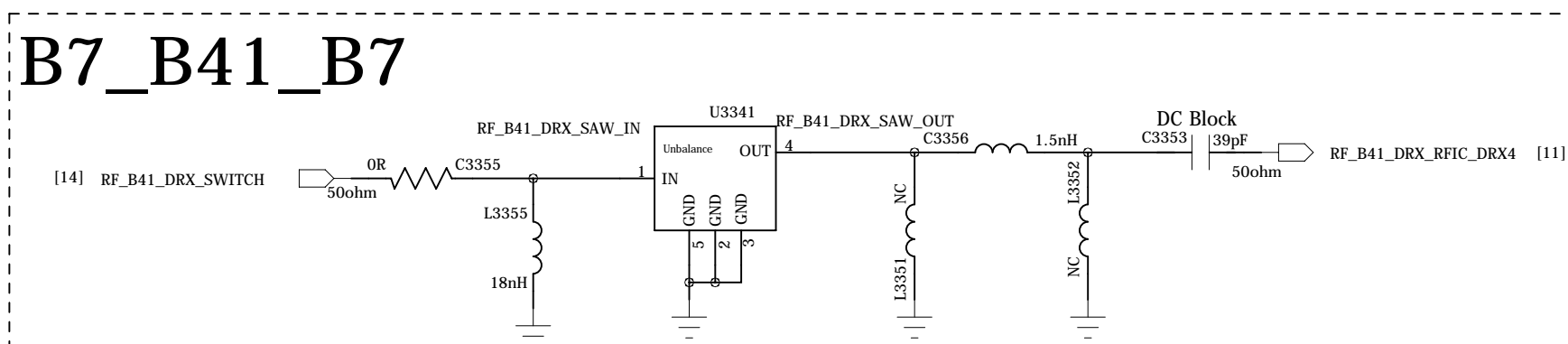
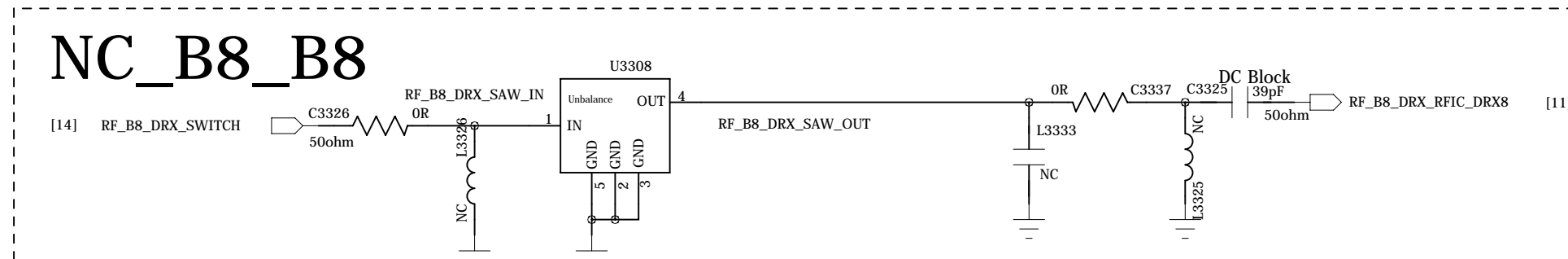
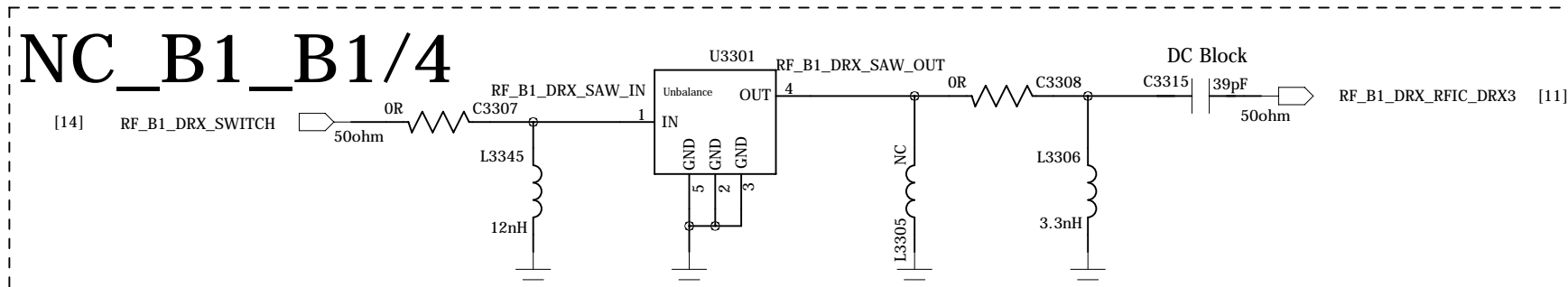
VC16I3 control logic				
VC1	VC2	RF1	RF2	RF3
H	L	Y	N	N
H	H	N	Y	N
N	H	N	N	Y

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Power

```

graph LR
    A((VFE28_PMU)) --- B(( ))
    B --- C((VFE28_PMU 0.2mm))
    B --- D[1uF C3303]
    D --- GND[ ]
  
```

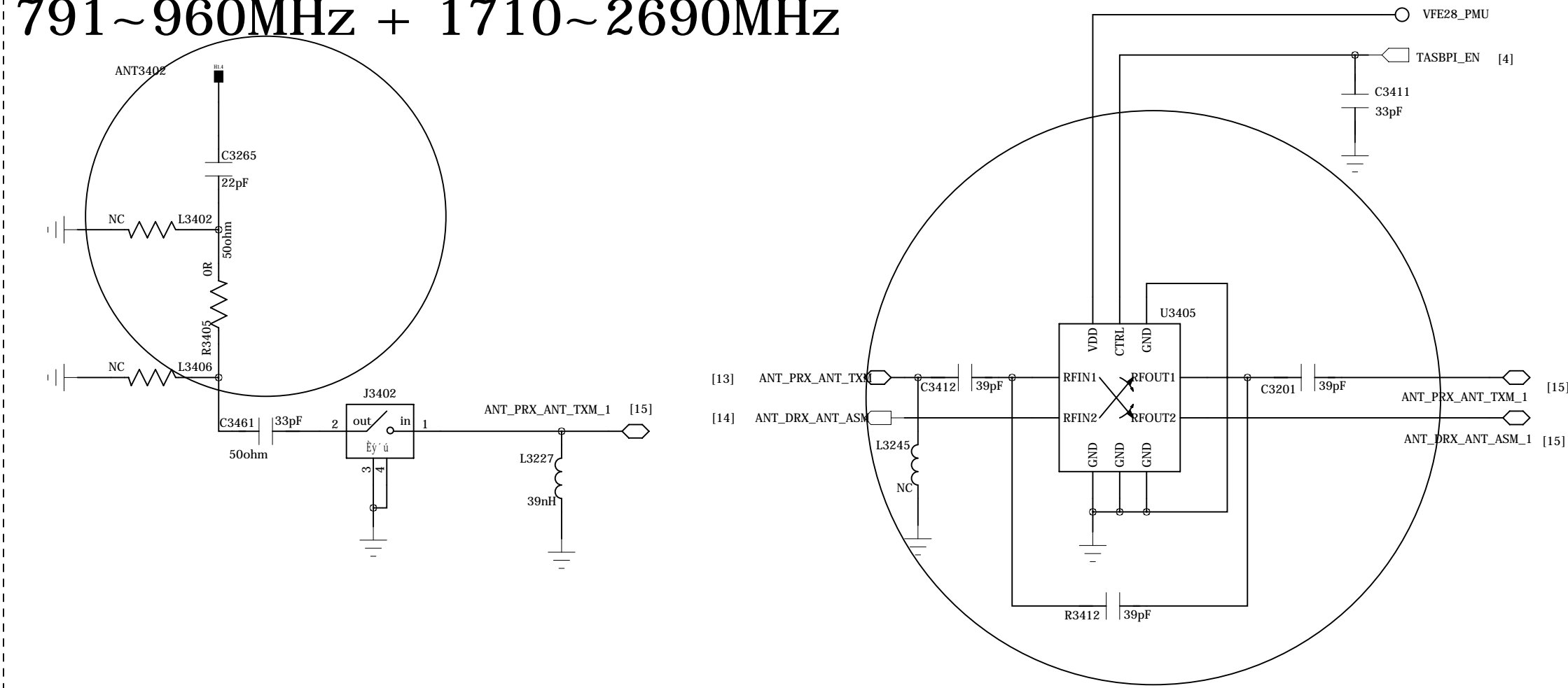


COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 33_RF_MT6177M_RF_DRX		VERSION: V1.2	SHEET: 14 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

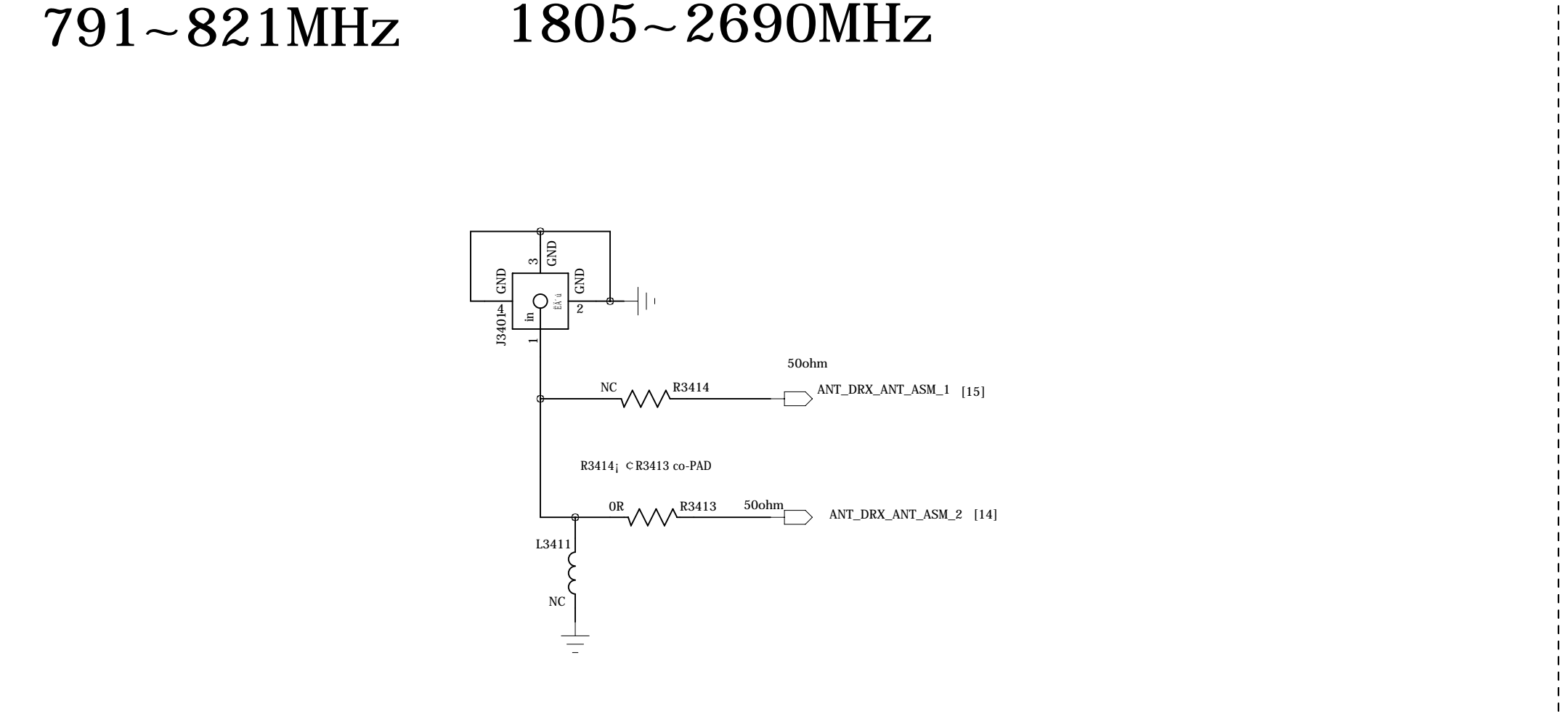
RF_MT6177M_RF_ANT

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

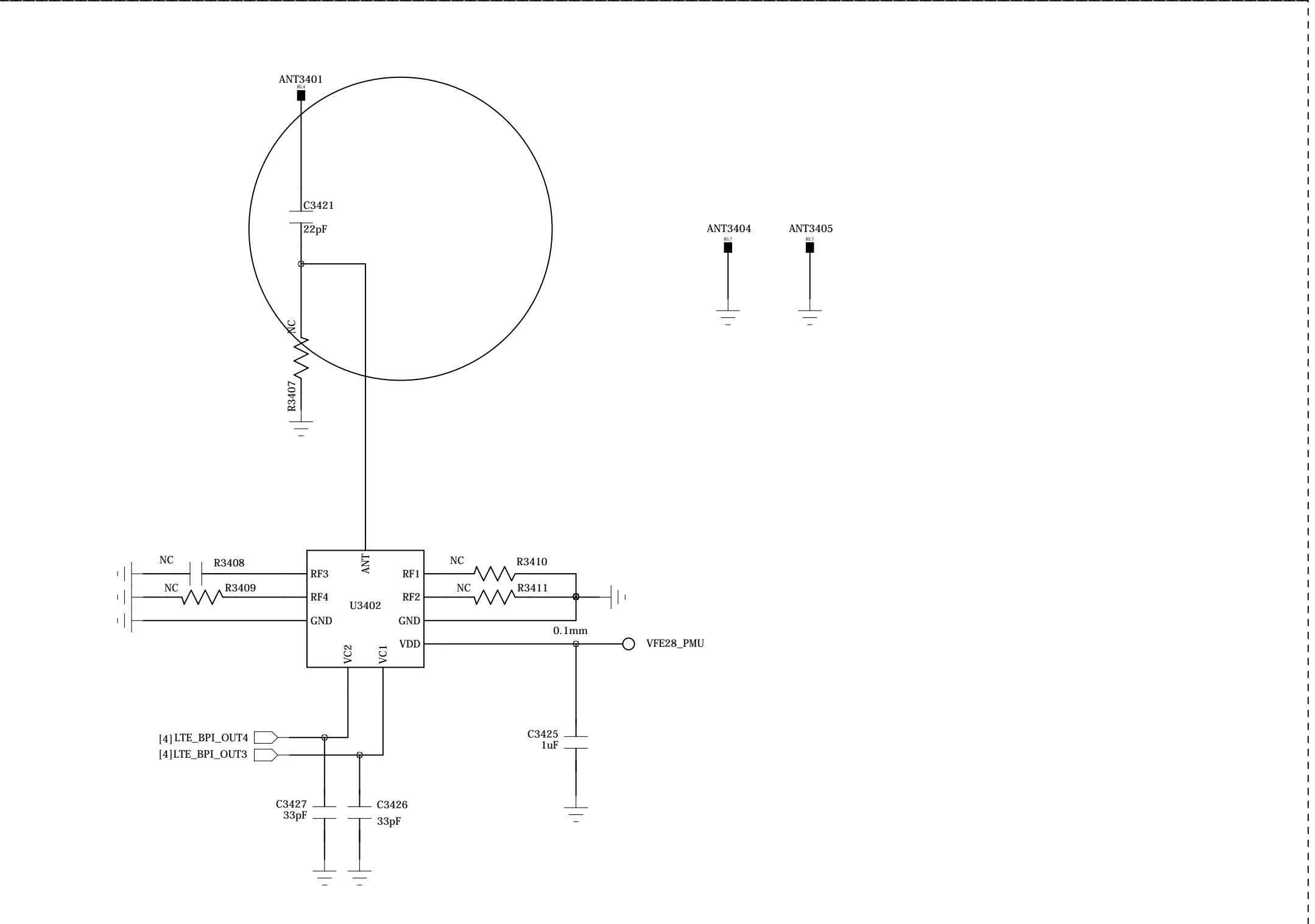
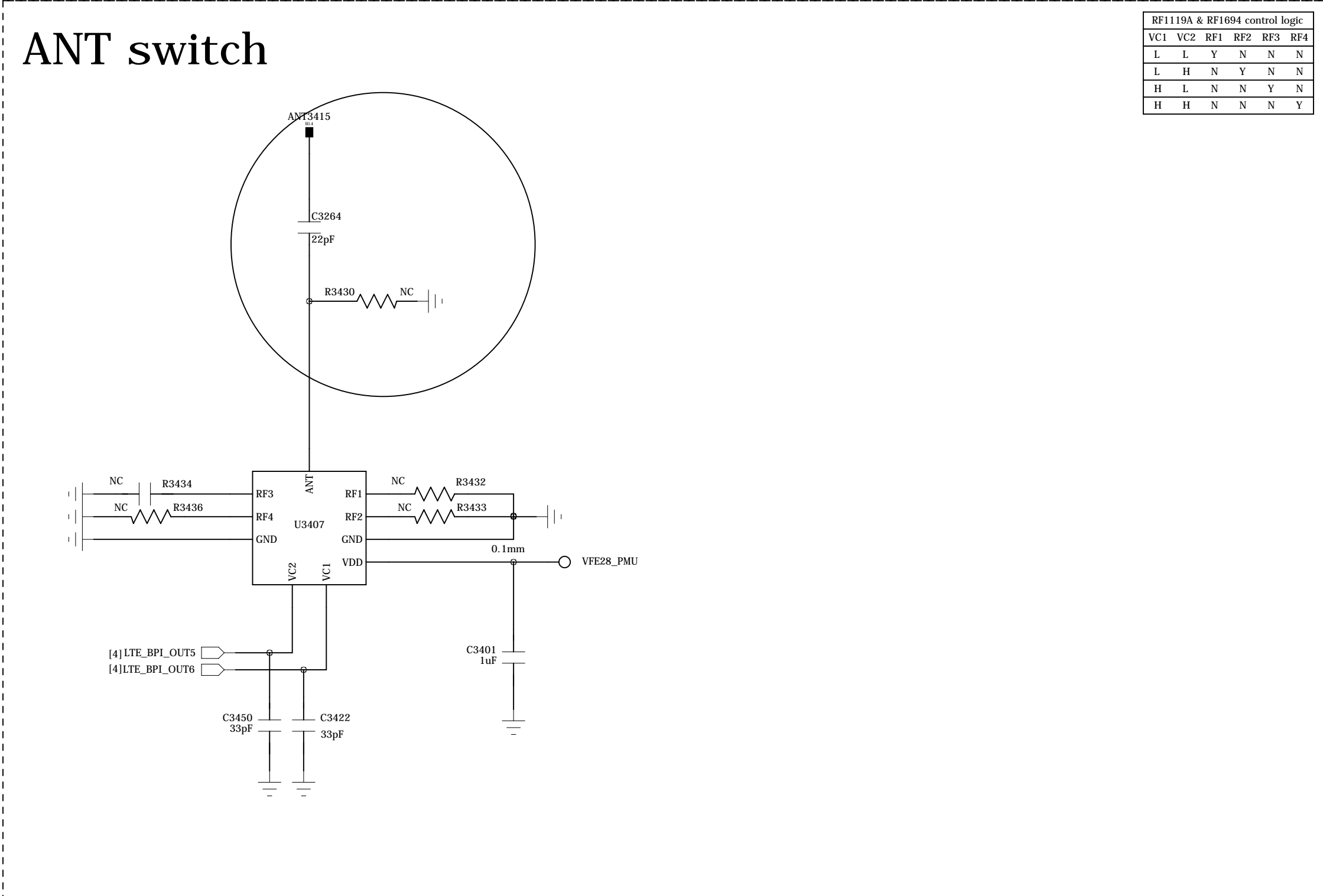
ASM_Main
791~960MHz + 1710~2690MHz



DRX ANT
791~821MHz 1805~2690MHz



ANT switch

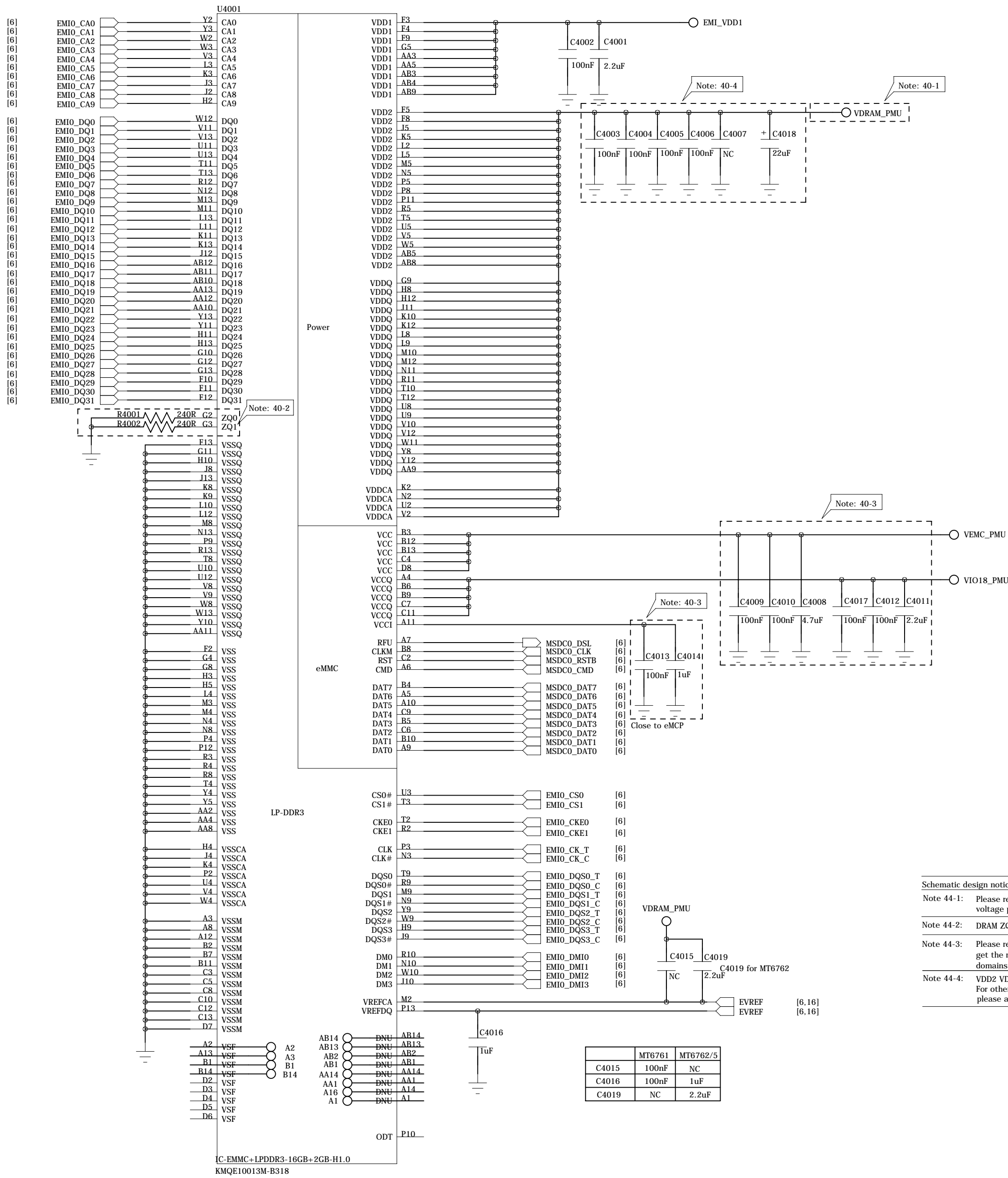


RF1119A & RF1694 control logic						
VC1	VC2	RF1	RF2	RF3	RF4	
L	L	Y	N	N	N	
L	H	N	Y	N	N	
H	L	N	N	Y	N	
H	H	N	N	N	Y	

COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 34_RF_ANT_CONTROLLER		VERSION: V1.2	SHEET: 15 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

MEMORY_eMMC_LPDDR3

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

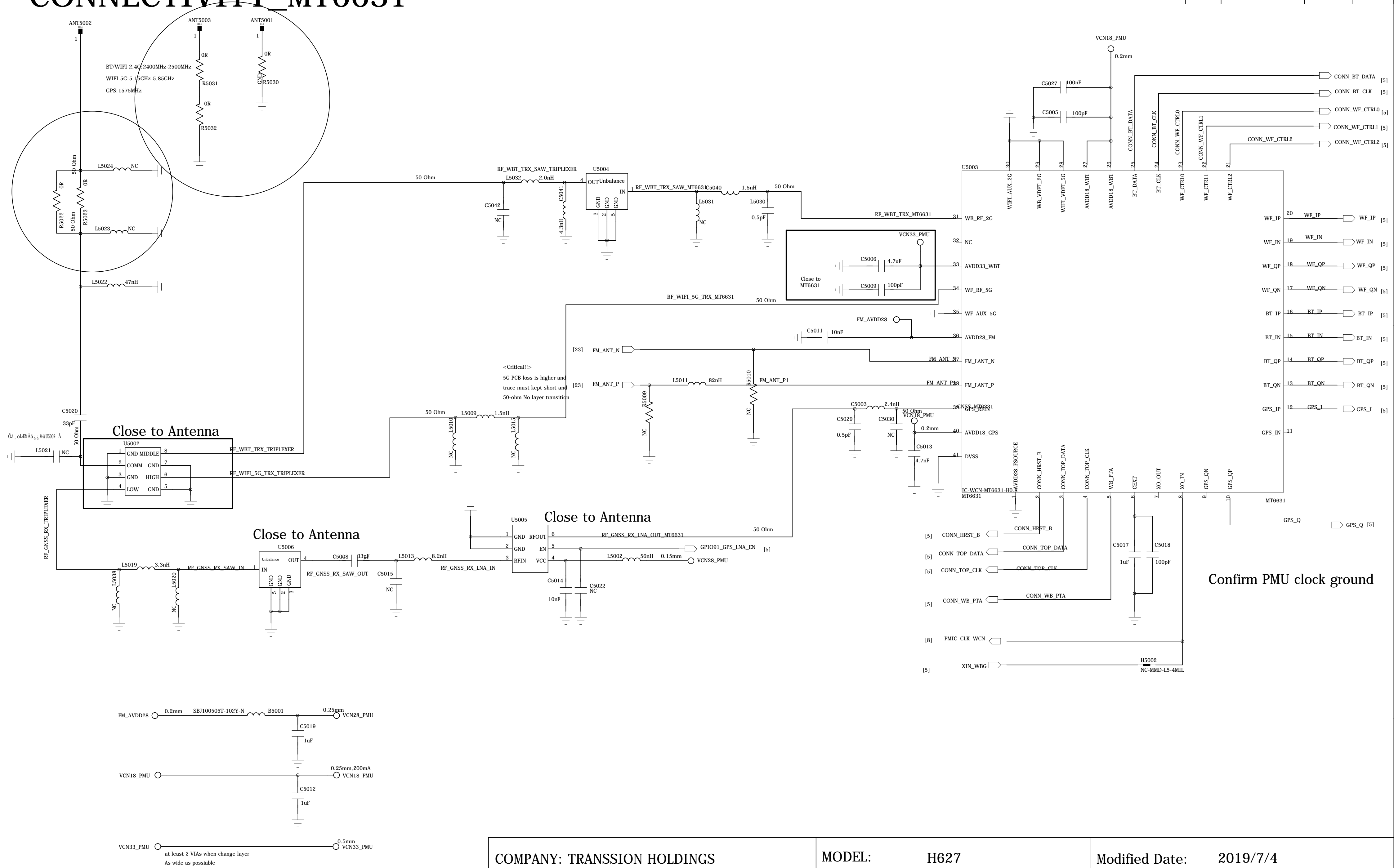


Schematic design notice of "44_Memory_eMMC_LPDDR3"	
Note 44-1:	Please refer to power supply related page select VDRAM1 output voltage properly for LPDDR3
Note 44-2:	DRAM ZQx resistor = 240ohm (1%) that must be connected to GND
Note 44-3:	Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDD1 power domains of eMMC.
Note 44-4:	VDD2 VDDQ VDDCA decoupling cap: closed to DRAM ball. For other cap for PMIC (>10uF, at PMIC page); please also refer to MMD and layout guide for placement.

COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 40_MEMORY_EMMC_LPDDR3		VERSION: V1.2	SHEET: 16 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

CONNECTIVITY_MT6631

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



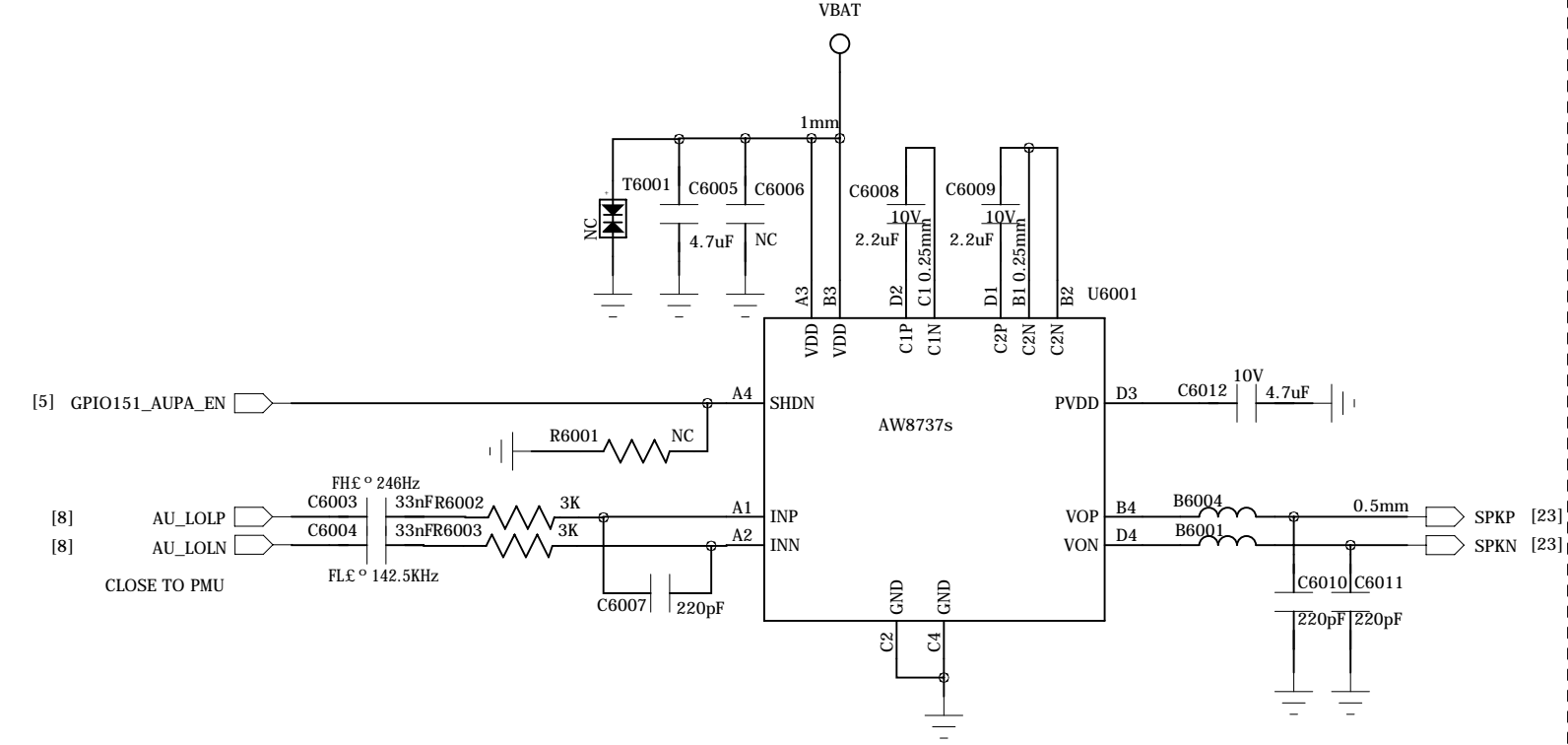
Confirm PMU clock ground

COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 50_CONNECTIVITY_MT6631		VERSION: V1.2	SHEET: 17 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

Star Power

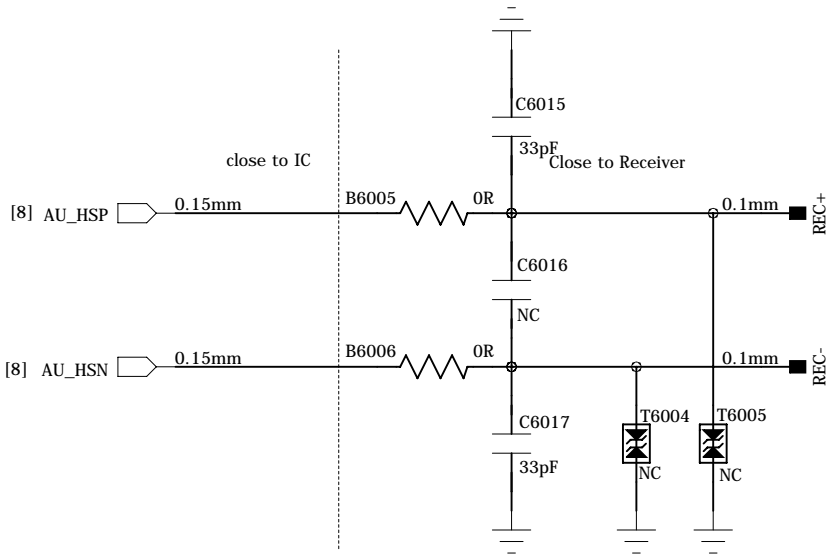
PERI_AUDIO_IO

Audio PA

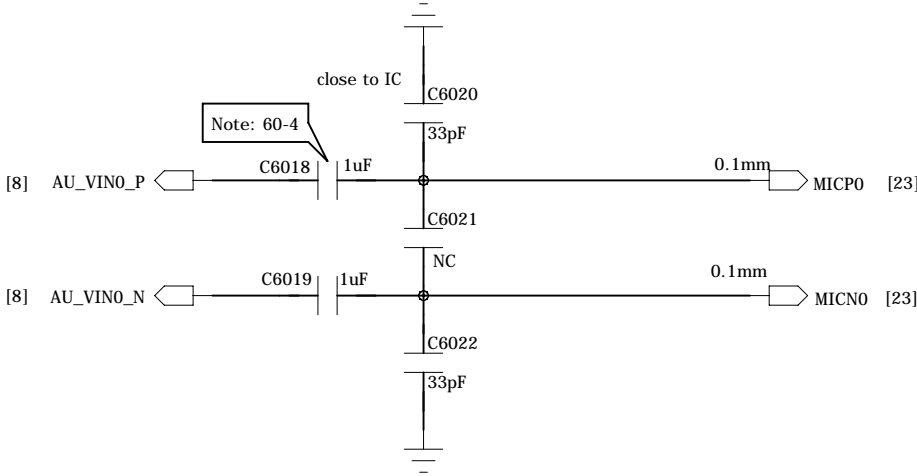


SUB MICPHONE

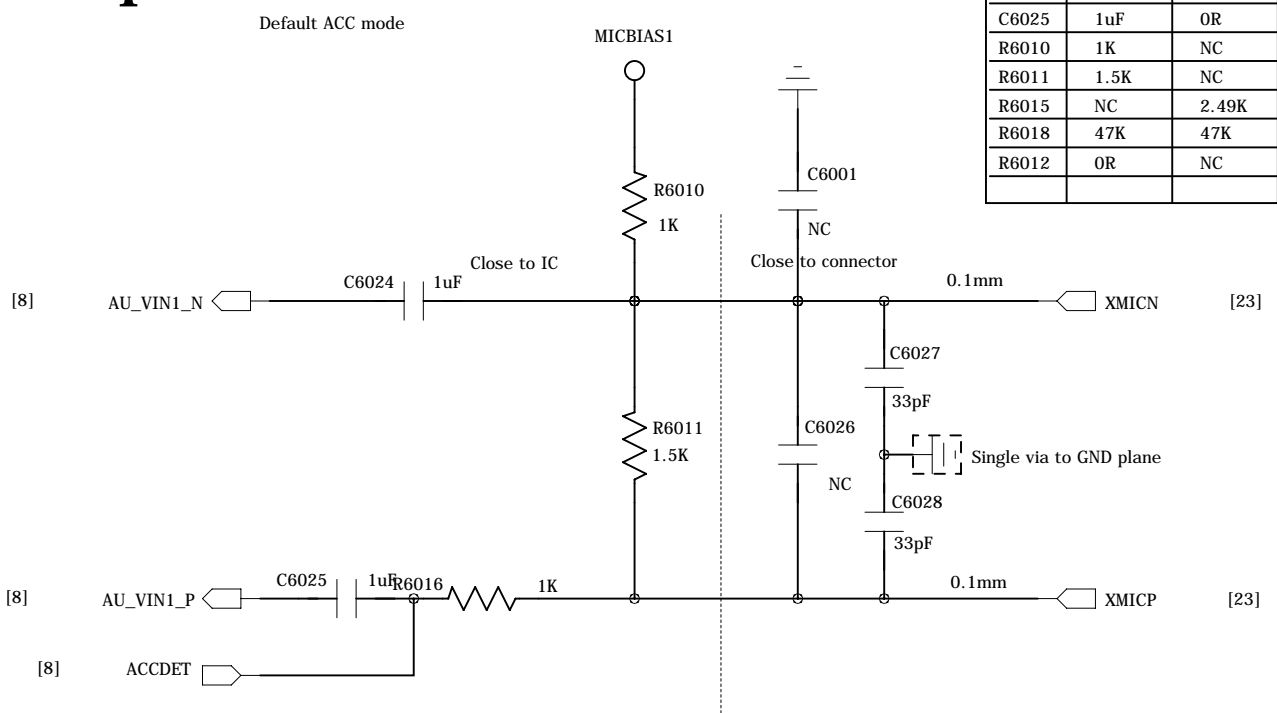
Receiver



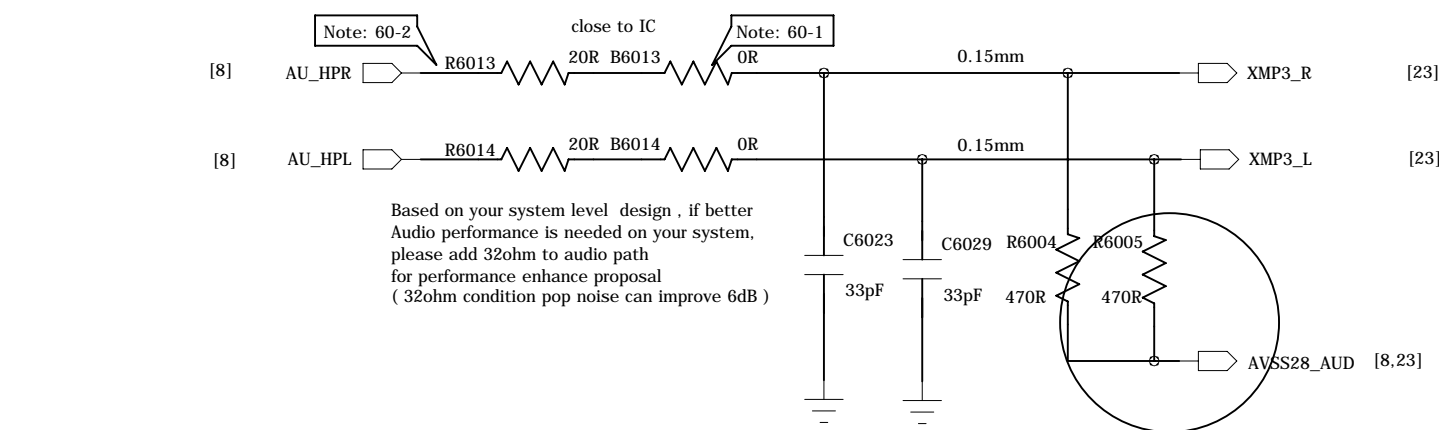
Main MICPHONE



Earphone MICPHONE



Earphone Receiver



Schematic design notice of "60_PERI_AUDIO_IO" page.

Note 60-1: B6009 B6010 B6013 B6014 needs change to "BLM18BD102SN1" for high THD performance(-90dB), but this BOM change will result in FM RSSI 10dB degraded.

Note 60-2: To reserve a resistor in HPL and HPR in series connection both in order to optimize headphone pop noise. The recommended value of this resistor is 33R.

Note 60-3: Layout trace from MT8353 ball J3 AUDREFN to Audio jack GND must surround shield with GND.

Note 60-4: 0.1/1uF for ACC mode(1uF for WB_AMR Speech/0.1uF for NB_AMR Speech),OR for DCC mode.

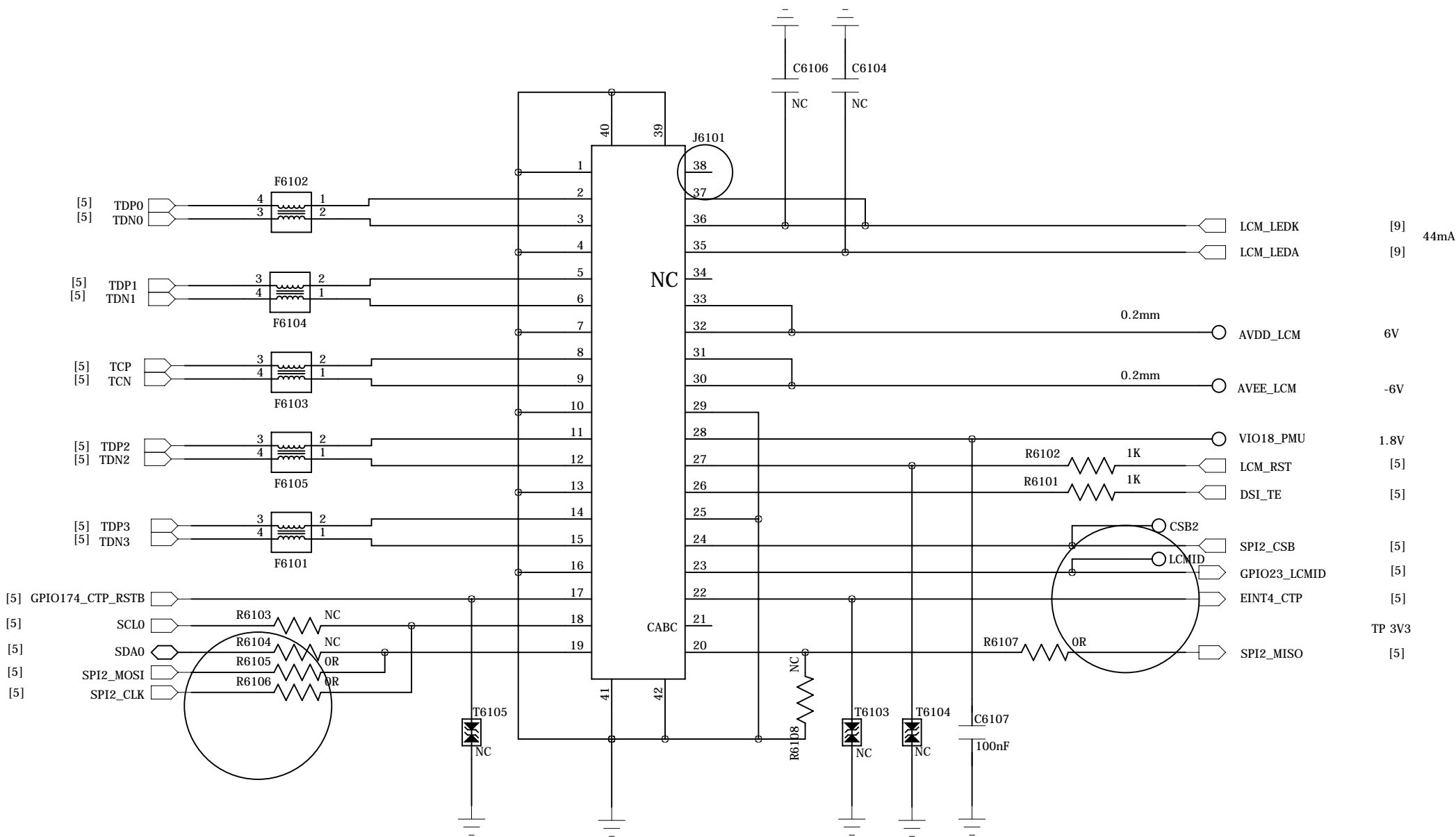
COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 60_PERI_AUDIO		VERSION: V1.2	SHEET: 18 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

PERI_LCM_CTP_FP

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

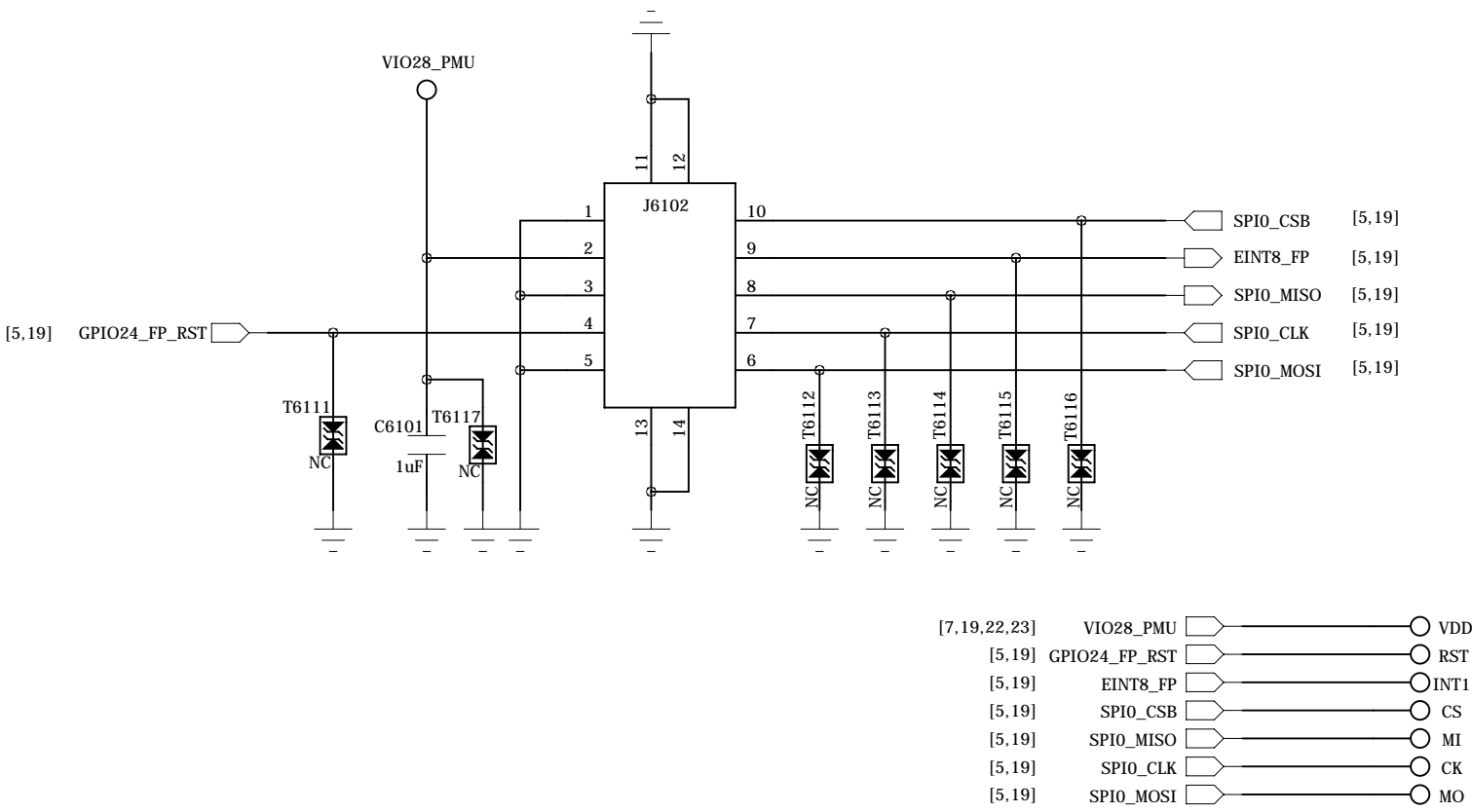
LCD_CTP_INTERFACE 6.55 Hole HD+

CTP (NT36525) I2C address: 0X01 (Write:0x02, Read:0x03)



	R6103	R6104	R6105	R6106	R6107	R6108	
normal	OR	OR	NC	NC	NC	OR	
no flash TP	NC	NC	OR	OR	OR	NC	

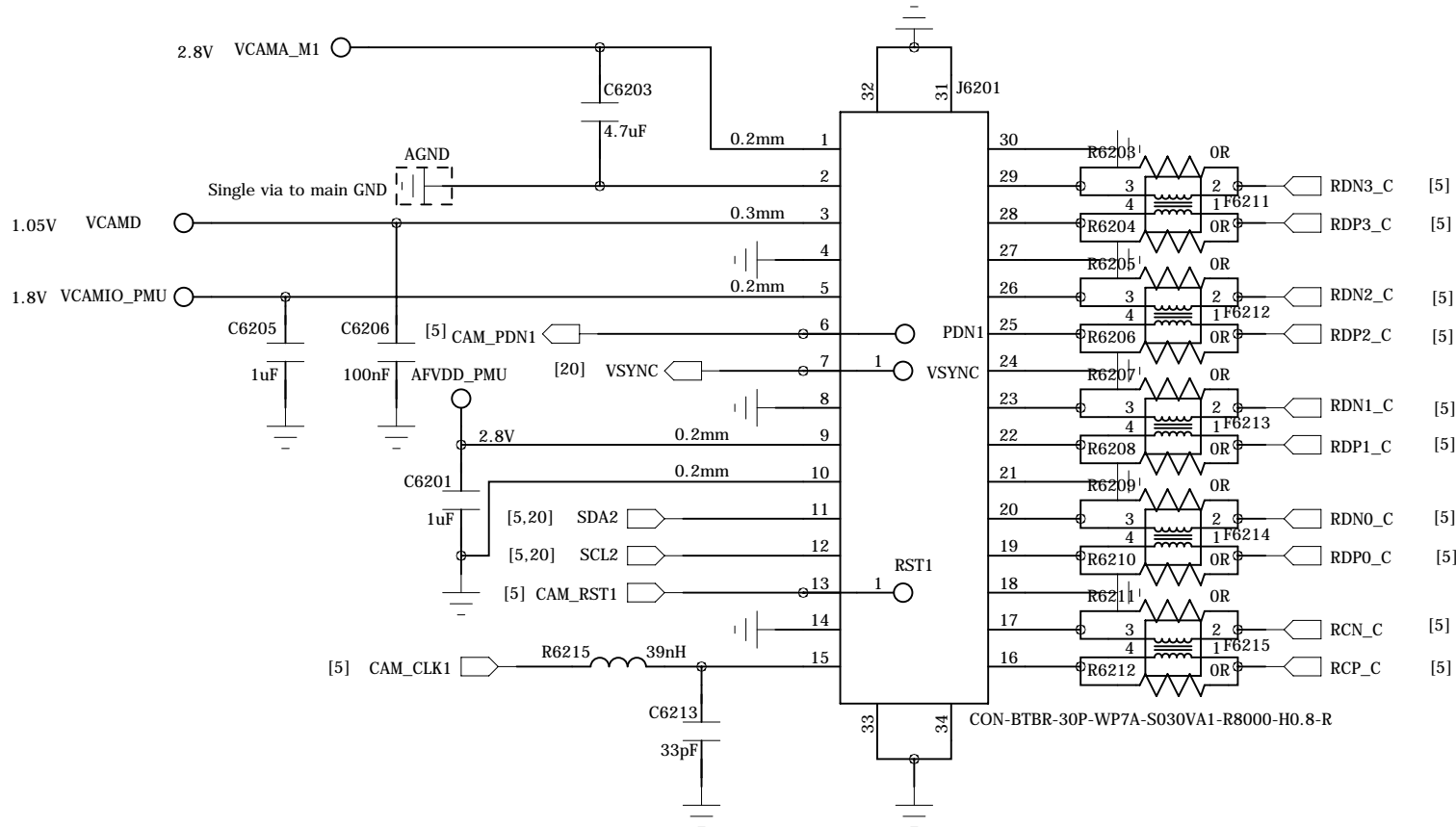
FINGER PRINT



COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 61_PERI_LCM_CTP_FP		VERSION: V1.2	SHEET: 19 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

PERI_REAR_CAMERA

REAR CAMERA Wide (13M/16M/48M+AF)

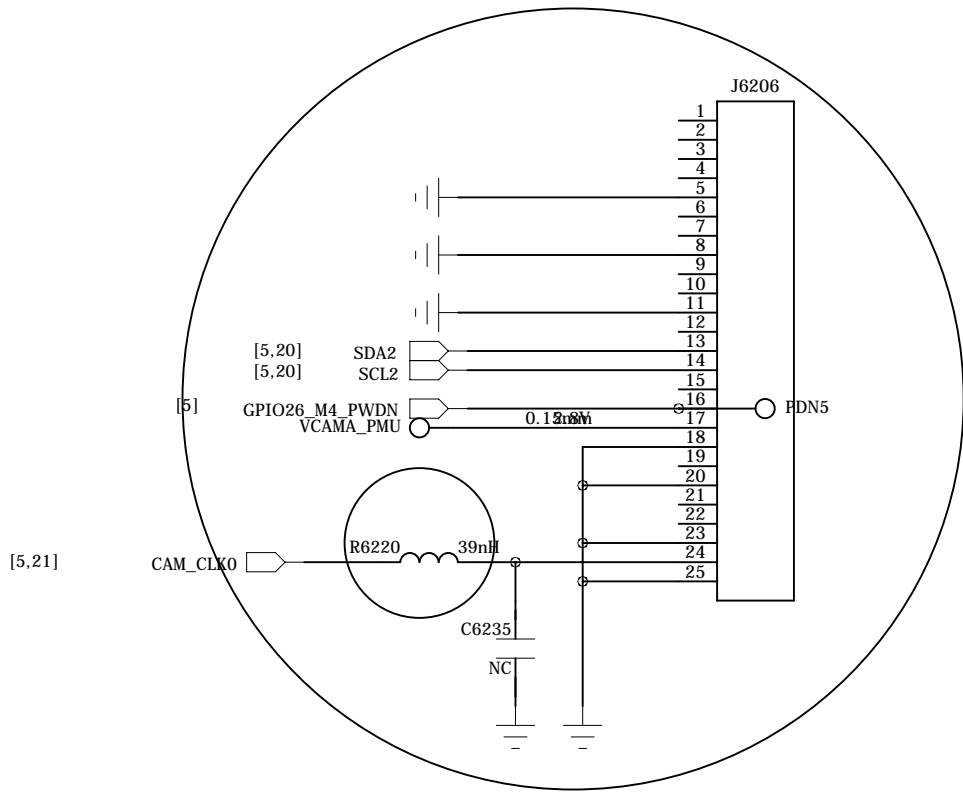


SENSOR	VCAMA	VCAMD	VCAMIO	AFVDD
S5K3L6XX03-FGX9	2.8V 60mA	1.05V 200mA	1.8V 1mA	2.8V 100mA
S5K3P9SX04-FGX9	2.8V 57.85mA	1.05V 166.01mA	1.8V 0.65mA	2.8V 100mA
S5KGM1SP03-FGX9	2.8V 55mA	1.05V 190mA	1.8V 1mA	2.8V 100mA

		SENSOR	I2C Address
48M		SENSOR(S5KGM1SP03-FGX9)	Write:0x20 Read:0x21
		MOTOR(GT9761-CL1-TR)	Write:0x18 Read:0x19
		EEPROM(BL24SA64-CS)	Write:0xA0 Read:0xA1
16M		SENSOR(S5K3P9SX04-FGX9)	Write:0x20 Read:0x21
		MOTOR(FP5510EE4)	Write:0x18 Read:0x19
		EEPROM(BL24SA64-CS)	Write:0xA0 Read:0xA1
13M	Sunvin	SENSOR(S5K3L6XX03-FGX9)	Write:0x20 Read:0x21
		MOTOR(DW9718S)	Write:0x18 Read:0x19
		EEPROM(P24C64E-C4H-MIR)	Write:0xA0 Read:0xA1
	SHINETECH	SENSOR(S5K3L6XX03-FGX9)	Write:0x20 Read:0x21
		MOTOR(DW9718S)	Write:0x18 Read:0x19
		EEPROM(BL24SA64-CS)	Write:0xA0 Read:0xA1

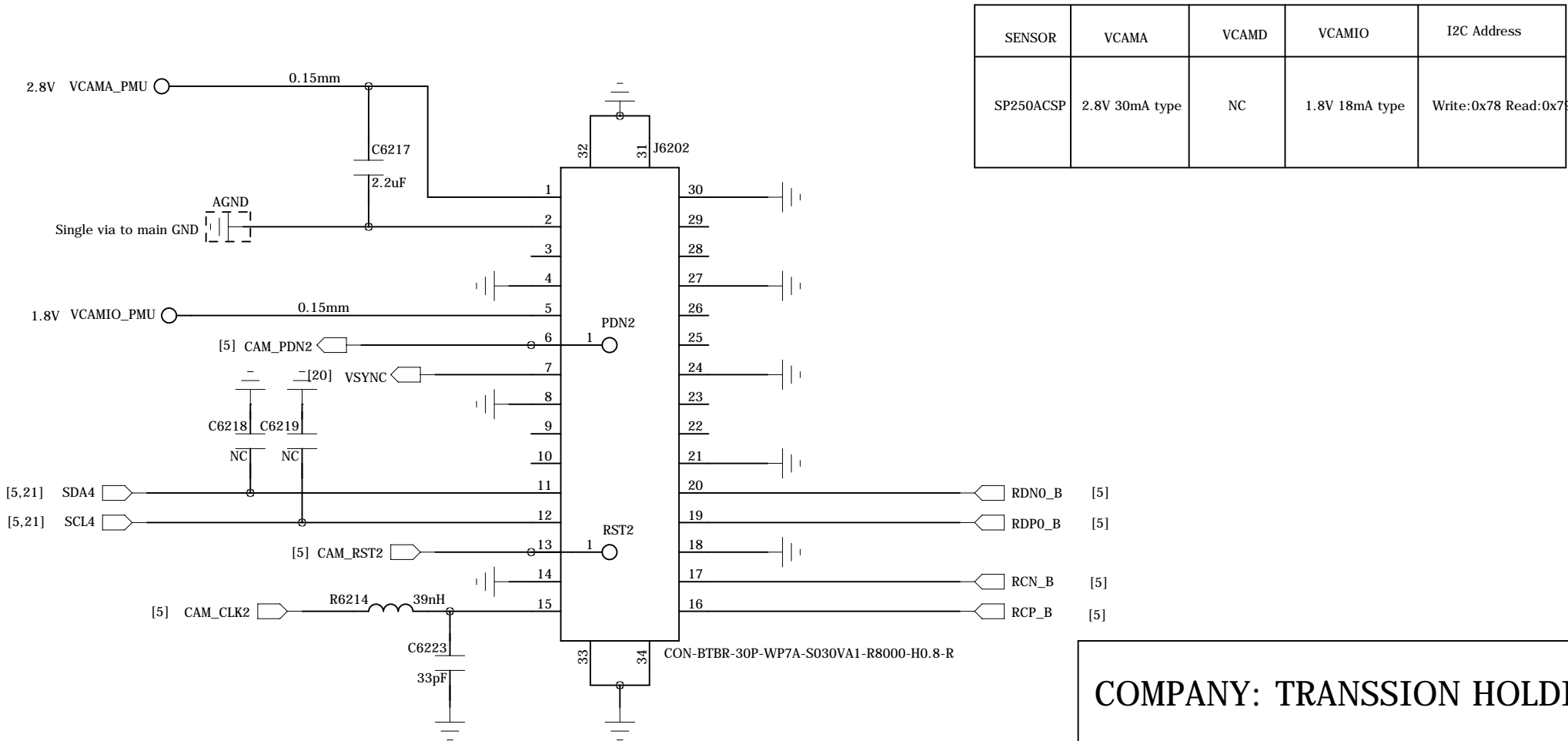
REAR 4 CAMERA (8W)

SENSOR	VCAMA	VCAMIO	I2C Address
GC6153	2.8V 20mA	NC	Write:0x80 Read:0x81



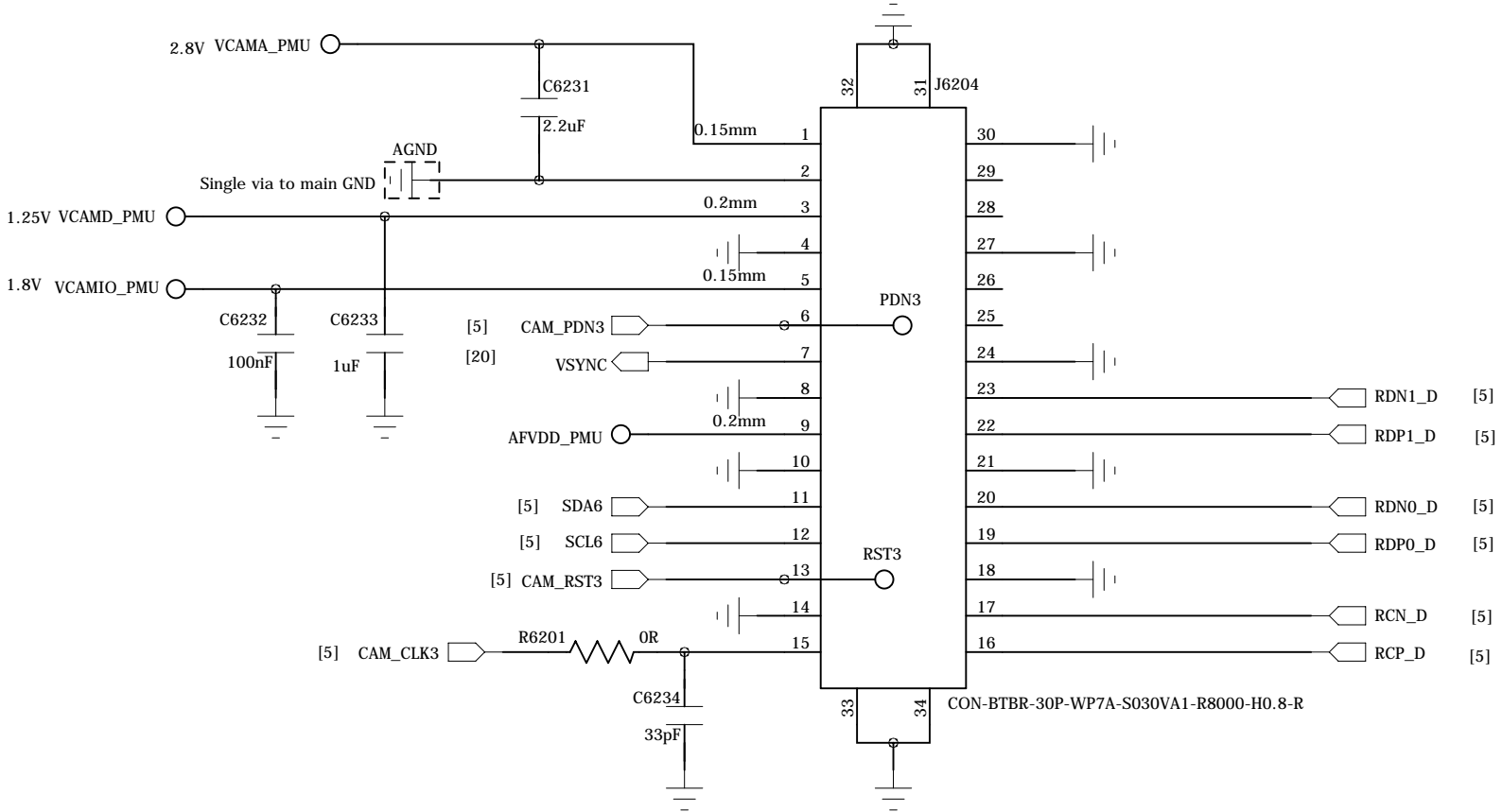
SENSOR	VCAMA	VCAMD	VCAMIO	VCAMAF	I2C Address
GC8034W	2.8V 35mA	1.25V 140mA	1.8V 10mA	2.8V 120mA	Write:0x6E Read:0x6F
S5K4H7YX04-FGX9	2.8V 30mA	1.2V 96.5mA	1.8V 43mA	2.8V 100mA	Write:0x20 Read:0x21
P24C64E-C4H-MIR					Write:0xA0 Read:0xA1
FP5510EE4					Write:0x18 Read:0x19
GC5035	2.8V 35mA	1.2V 80mA	1.8V 3mA	2.8V 120mA	Write:0x6E Read:0x6F

REAR CAMERA MONO (2M+FF)



SENSOR	VCAMA	VCAMD	VCAMIO	I2C Address
SP250ACSP	2.8V 30mA type	NC	1.8V 18mA type	Write:0x78 Read:0x79

REAR CAMERA Ultrawide (5M/8M+AF)



COMPANY: TRANSSION HOLDINGS

MODEL: H627

Modified Date: 2019/7/4

DRAWN

DJF/TS

DATED

20190603

TITLE: 62_PERI_REAR_CAMERA

VERSION: V1.2

SHEET: 20 OF 24

CHECKED

<CHECKED>

DATED

< >

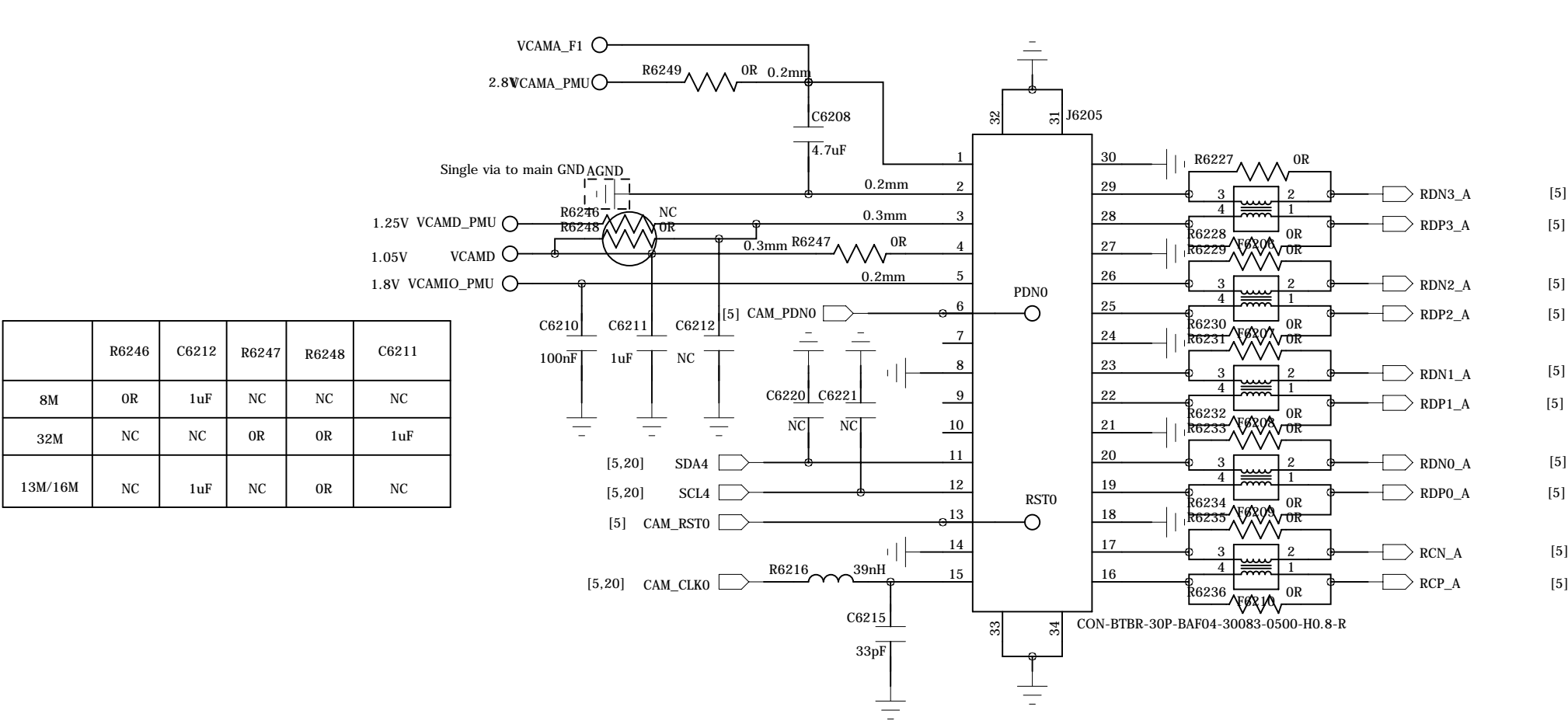
Confidentiality

CONFIDENTIAL

PERI_FRONT_CAMERA

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

FRONT MAIN CAMERA (MAX 32M+ FF)



	R6246	C6212	R6247	R6248	C6211
8M	OR	1uF	NC	NC	NC
32M	NC	NC	OR	OR	1uF
13M/16M	NC	1uF	NC	OR	NC

	SENSOR	I2C Address
32M	S5KGD1SP03-FGX9 P24C64E-C4H-MIR	Write:0x5A Read:0x5B Write:0xA2 Read:0xA3
8M	GC8034	Write:0x6E Read:0x6F
13M	S5K3L6XX03-FGX9 P24C64E-C4H-MIR	Write:0x5A Read:0x5B Write:0xA2 Read:0xA3
16M	S5K3P9SX04-FGX9 P24C64E-C4H-MIR	Write:0x5A Read:0x5B Write:0xA2 Read:0xA3

	SENSOR	VCAMA	VCAMD	VCAMIO
	S5KGD1SP03-FGX9	2.8V 75.4mA	1.05V 603.34mA	1.8V 20.11mA
	GC8034	2.8V 35mA	1.25V 140mA	1.8V 10mA
	S5K3L6XX03-FGX9	2.8V 60mA	1.05V 200mA	1.8V 1mA
	S5K3P9SX04-FGX9	2.8V 57.5mA	1.05V 159.9mA	1.8V 0.65mA

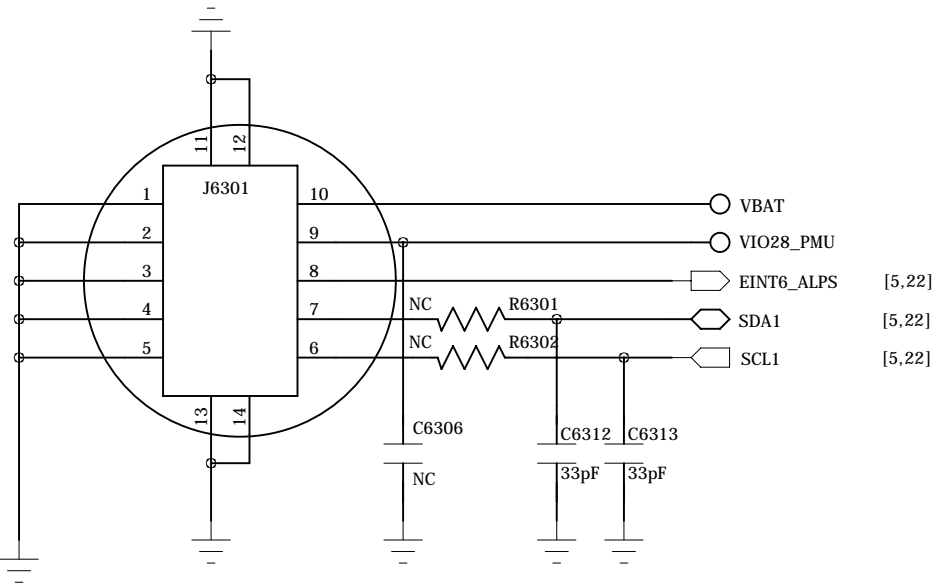
COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 62_PERI_FRONT_CAMERA		VERSION: V1.2	SHEET: 21 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

PERI_SENSORS

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

ALPS--FPC

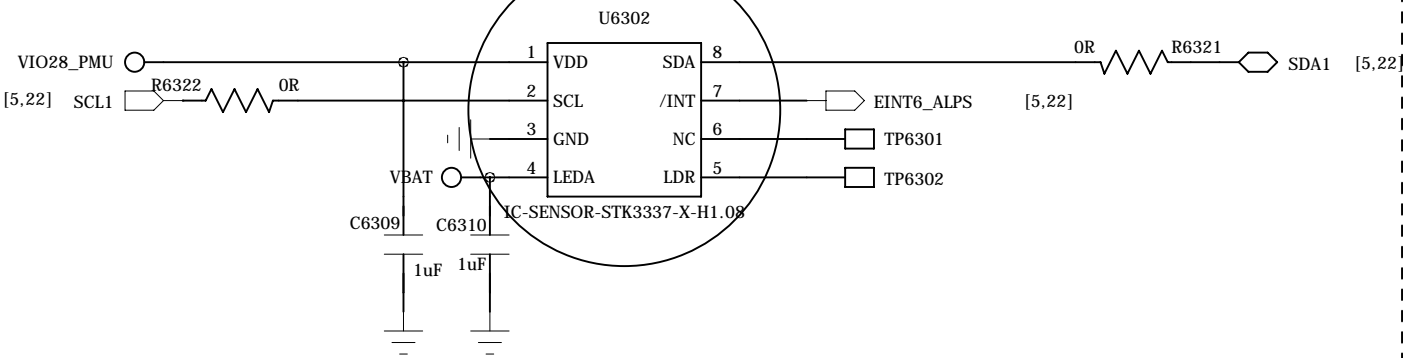
PA22C00001 address: Write:0x3C, Read:0x3D Default
STK3337-X: I2C address: Write:0x8E, Read:0x8F



Default	Reserve
U6302+U6307	J6301+U6307
STK3337-X CM32183A3OG	PA22C00001 CM32183A3OG

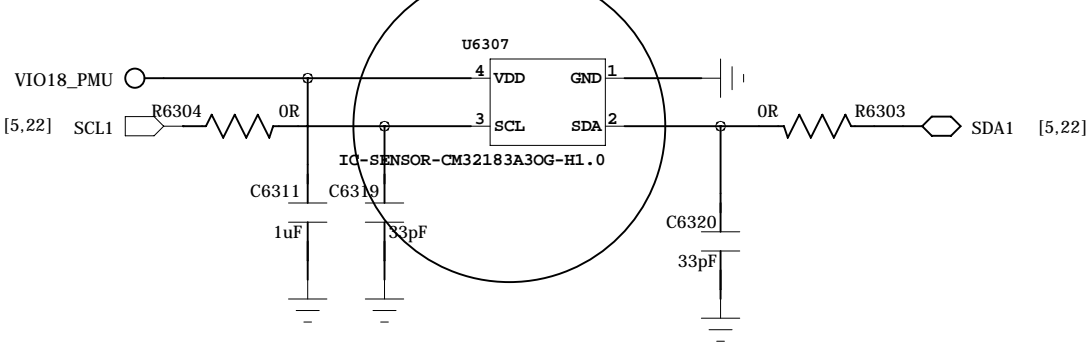
STK3337-X--ALPS-MB

STK3337-X: I2C address: Write:0x8E, Read:0x8F(Default)

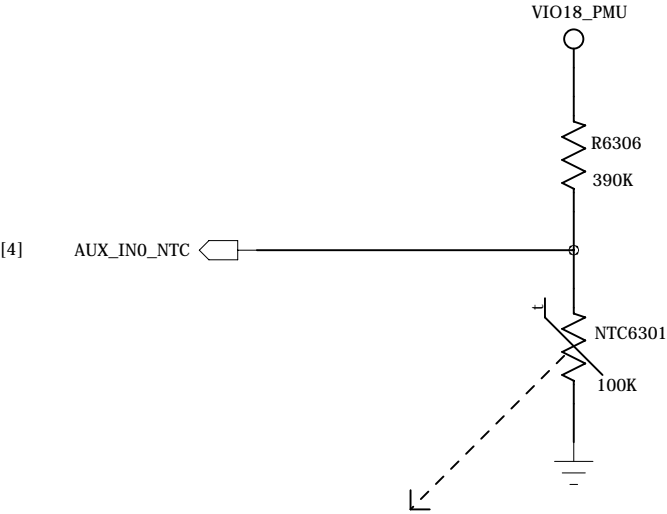


CM32183A30G--ALPS--FPC

CM32183A3OG: I2C address: Write:0x52, Read:0x53 Default



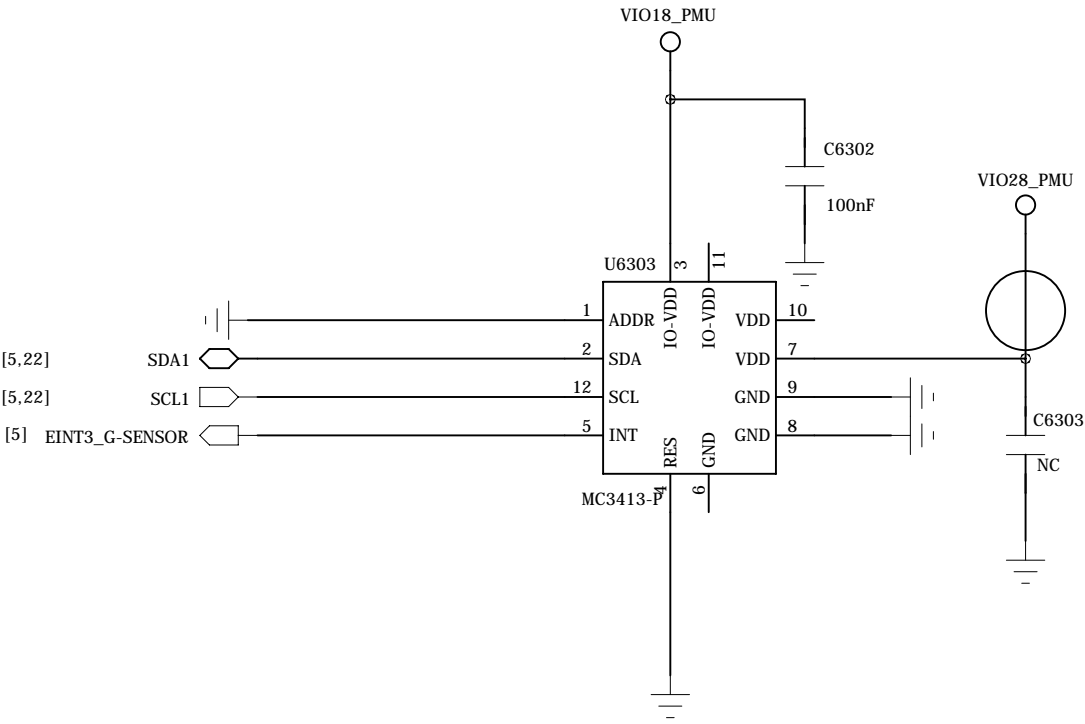
Thermistor to sense AP temperature



1. NTC6301 must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

G-Sensor

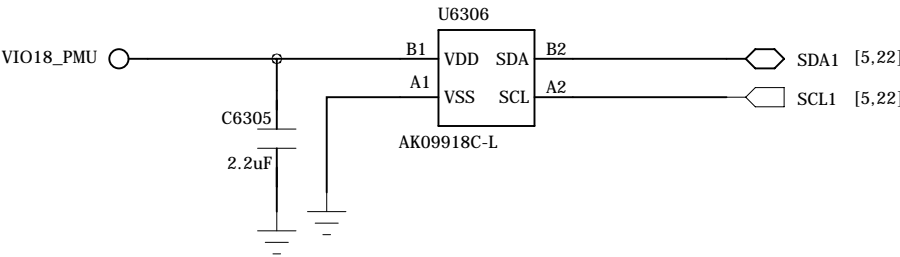
MC3416-P: ADDRESS: 0x98(Write)/0x99(Read) default
STK8BA50-S: ADDRESS: 0x30(Write)/0x31(Read) Reserve



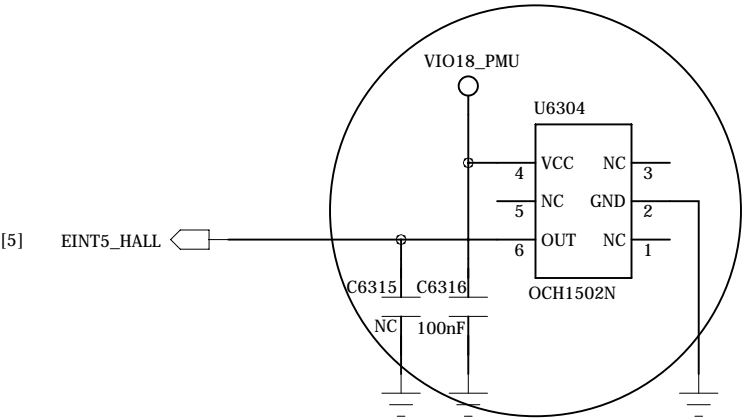
component	MC3416-P	STK8BA50-S
C6302	100nF	1uF
C6303	NC	1uF

M-Sensor (COMPASS)

AF6133: I2C ADDRESS: 0x18(Write)/0x19(Read) default
MMC5603NJL: I2C ADDRESS: 0x60(Write)/0x61(Read) Reserve



Unipolar HALL

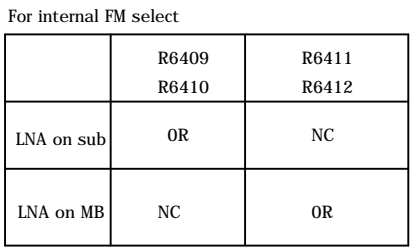


G-Sensor + Gyro Sensor

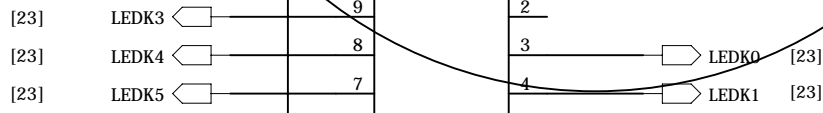
LSM6DS3TR-C: I2C address: Write:0xD4, Read:0xD5

COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 63_PERI_SENSORS		VERSION: V1.2	SHEET: 22 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



AW9106B:I2C address: Write:0xB6, Read:0xB7

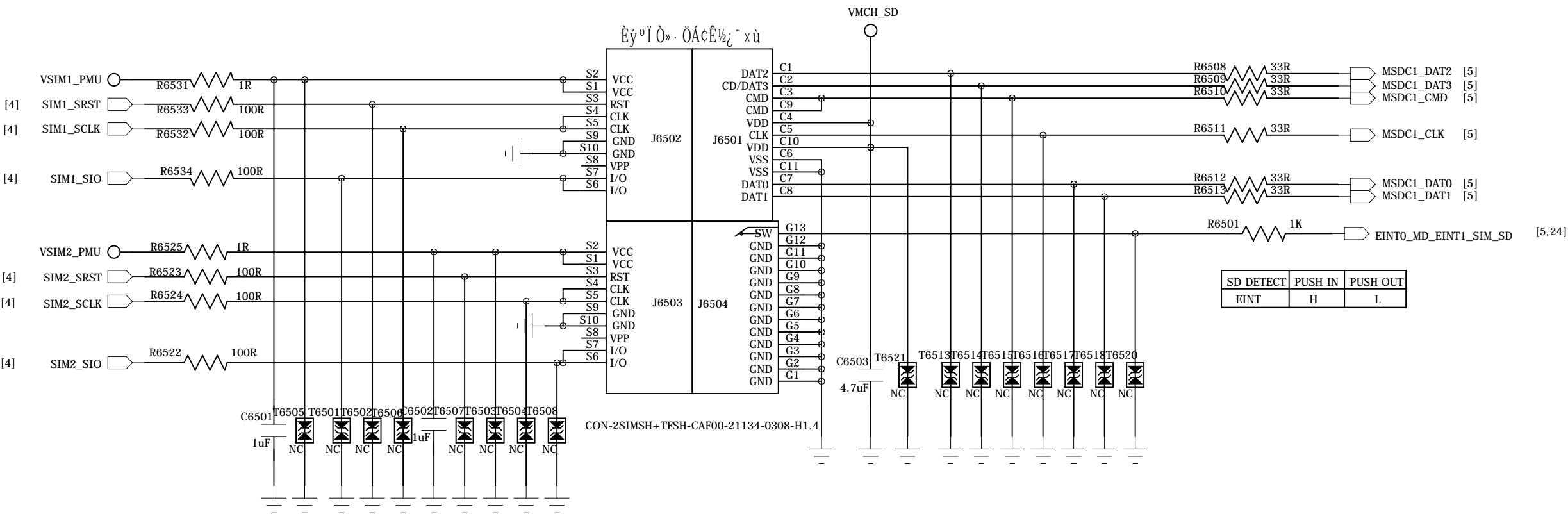
[illegible]

COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 64_PERI_IO_VIB_RGB_PDLC		VERSION: V1.2	SHEET: 23 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		

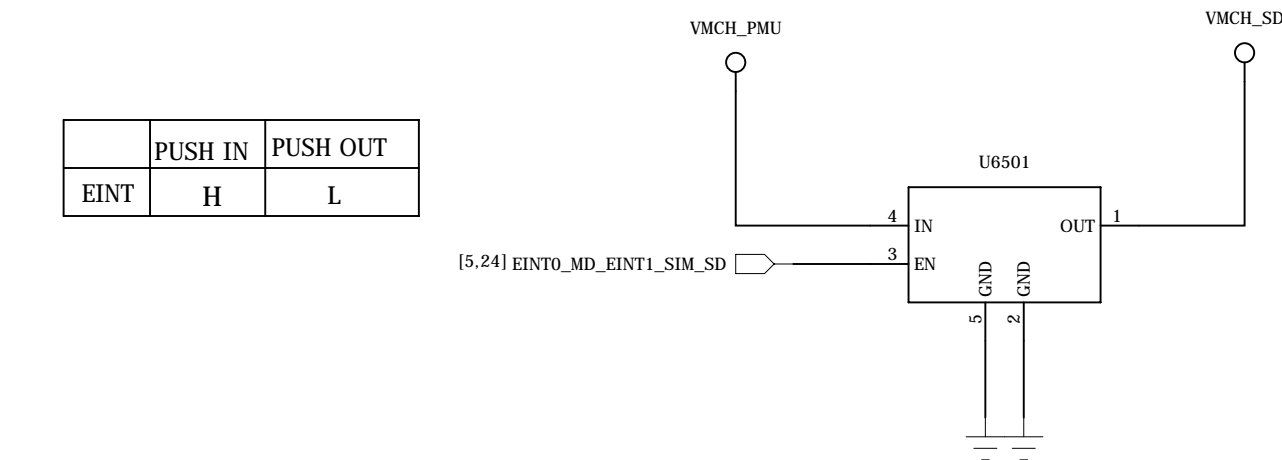
PERI_SIM_SD_LED

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

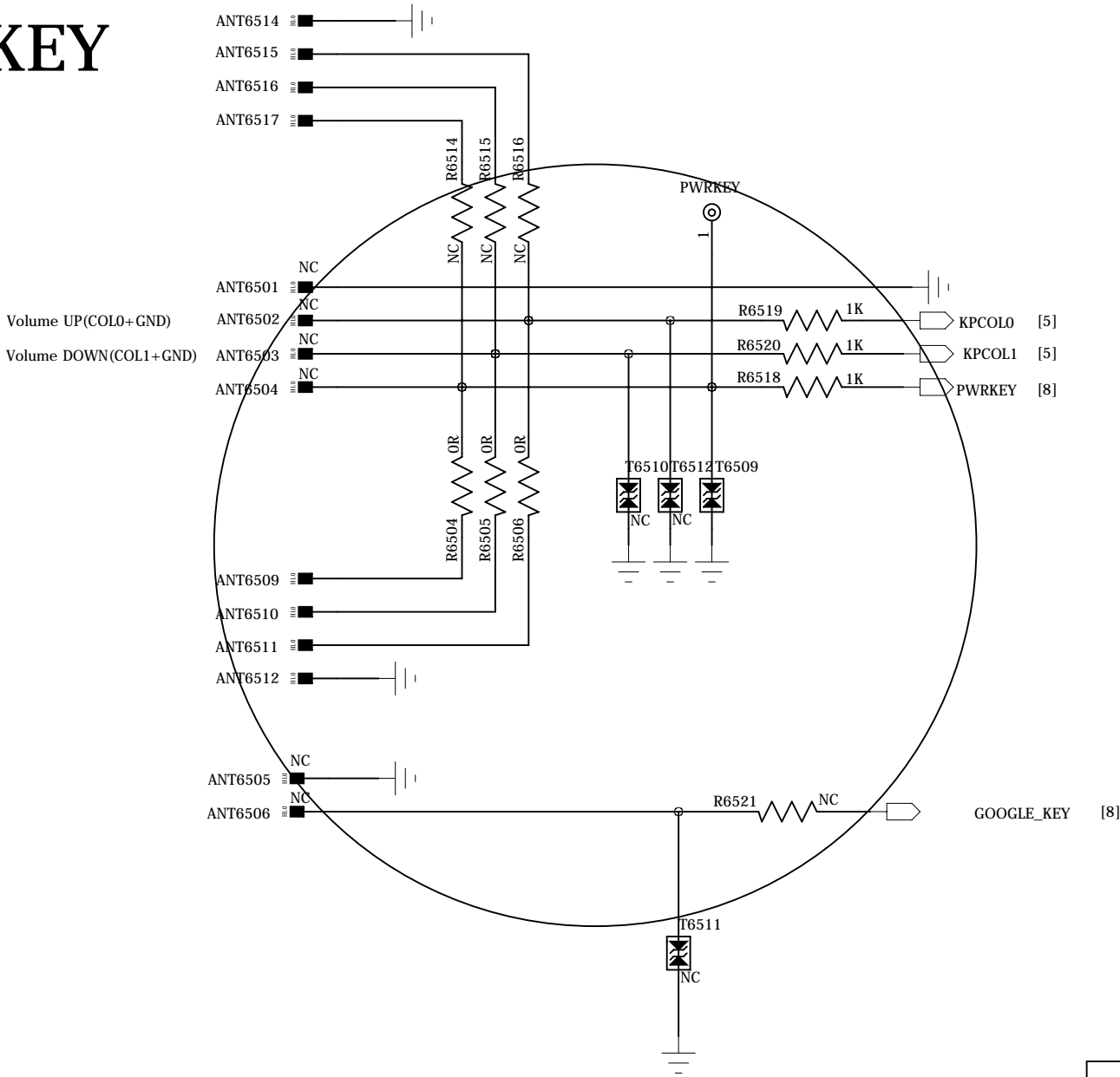
SIM/SD CARD



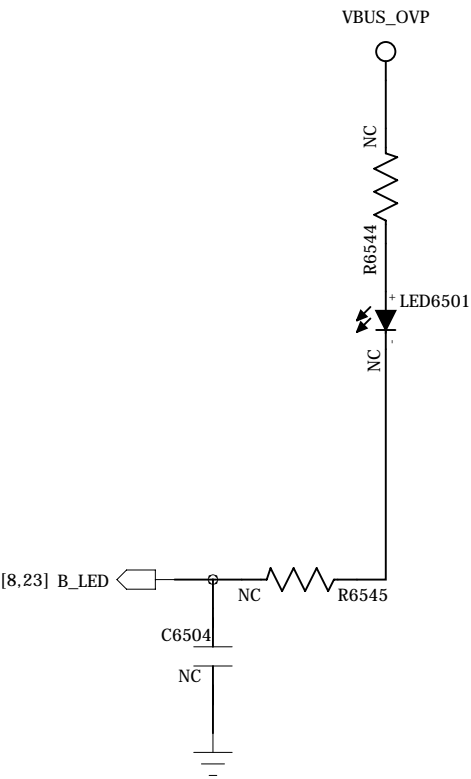
SD POWER CONTROL



SIDEKEY



Indicator LED1



COMPANY: TRANSSION HOLDINGS				MODEL: H627		Modified Date: 2019/7/4	
DRAWN	DJF/TS	DATED	20190603	TITLE: 65_PERI_SIM_SD_LED_SIDEKEY		VERSION: V1.2	SHEET: 24 OF 24
CHECKED	<CHECKED>	DATED	< >	Confidentiality	CONFIDENTIAL		